

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ✓ Surface-mounted package
- ✓ $T_j \text{ max } 175^\circ\text{C}$
- ✓ Advanced trench cell design
- ✓ MSL1

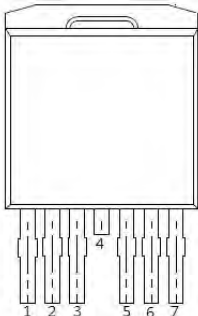
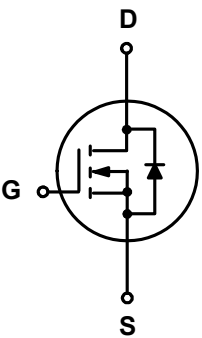
1.2 Applications

- ✓ LCD TV appliances
- ✓ LCDM appliances
- ✓ High power inverter system

1.3 Quick reference

- ✓ $BV \geq 120 \text{ V}$
- ✓ $P_{\text{tot}} \leq 333 \text{ W}$
- ✓ $I_D \leq 236 \text{ A}$
- ✓ $R_{\text{DS(ON)}} \leq 2.2 \text{ m}\Omega @ V_{\text{GS}} = 10 \text{ V}$
- ✓ $R_{\text{DS(ON)}} \leq 2.8 \text{ m}\Omega @ V_{\text{GS}} = 6 \text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)	 Top View TO-263-7L	
2,3	Source (S)		
4	Drain(D)		
5,6,7	Source (S)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _C = 25 °C	-	120	V
V _{GS}	Gate-Source Voltage	T _C = 25 °C	-	± 20	V
I _D *	Drain Current (DC)	T _C = 25 °C, V _{GS} = 10 V	-	236	A
		T _C = 100 °C, V _{GS} = 10 V	-	166	
I _{DM} **	Drain Current (Pulsed)	T _C = 25 °C, V _{GS} = 10 V	-	944	A
P _{tot}	Drain power dissipation	T _C = 25 °C	-	333	W
T _{stg}	Storage Temperature		- 55	175	°C
T _J	Junction Temperature		-	175	°C
I _S	Continuous-Source Current	T _C = 25 °C	-	236	A
E _{AS} *	Single Pulsed Avalanche Energy	V _{DD} = 50 V , L= 1.0 mH	-	2312	mJ
R _{θJA} *	Thermal Resistance- Junction to Ambient		-	40	°C/W
R _{θJC} *	Thermal Resistance- Junction to Case		-	0.45	

Notes :

* Surface Mounted on 1 in² pad area, t ≤ 10 sec

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

*** limited by bonding wire

4. Marking Information

Product Name	Marking
UP01N12D7	01N12 AYWW01 XXXXXX

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UP01N12D7	TO263-7L(D2-PAK)			800	

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

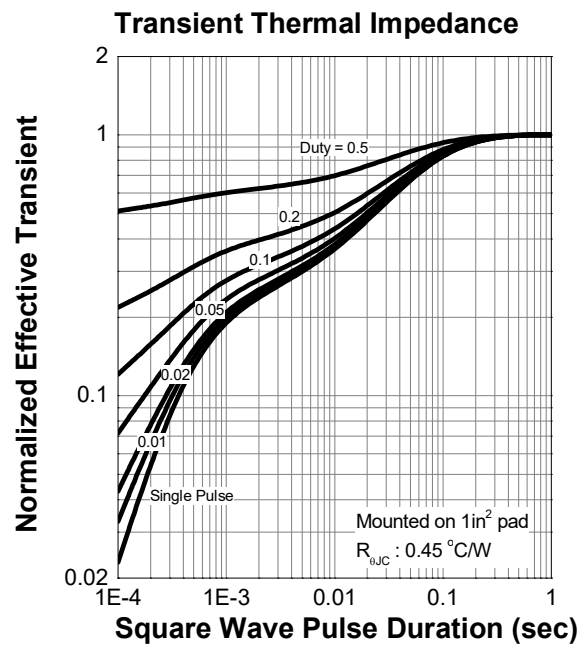
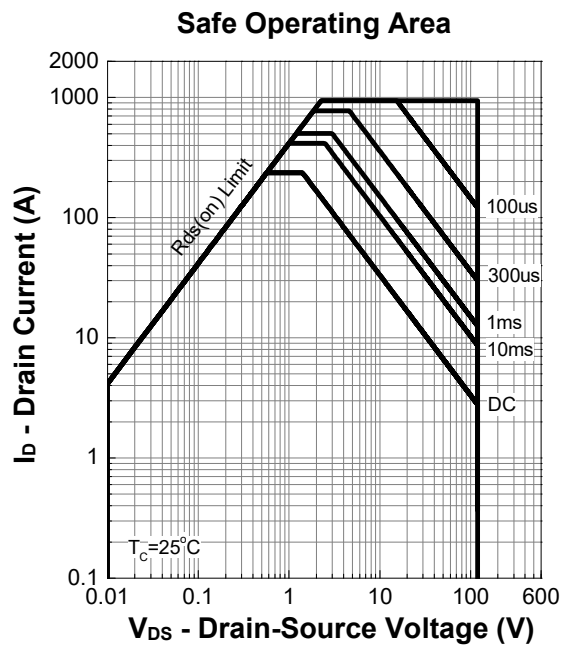
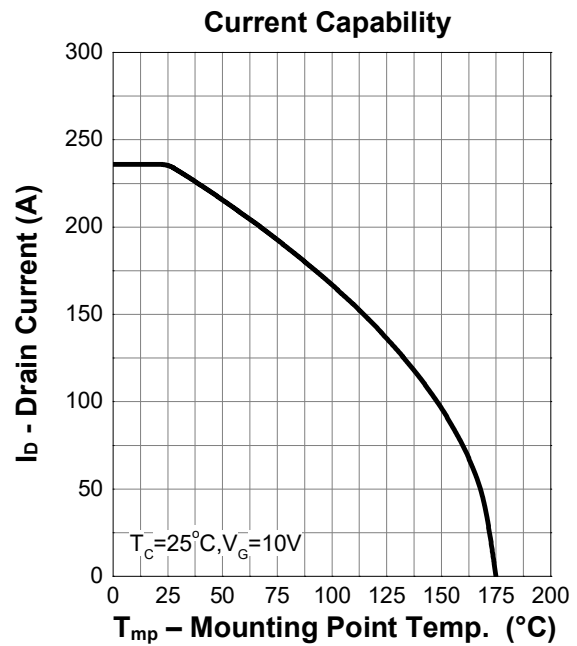
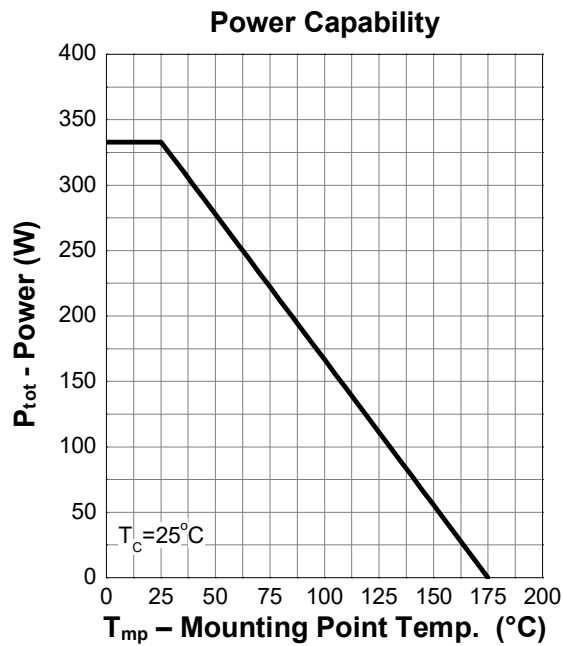
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	120	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	2	-	4	V
I _{DSS}	Drain Leakage Current	V _{DS} = 96 V, V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} = 10 V, I _{DS} = 50 A	-	2.0	2.2	mΩ
		V _{GS} = 6 V, I _{DS} = 30 A	-	2.4	2.8	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 50 A, V _{GS} = 0 V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _{DS} = 50 A, V _{GS} = 0 V dI _{SD} /dt = 100 A/μs	-	137	-	nS
Q _{rr}	Reverse Recovery Charge		-	462	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 60 V Frequency = 1 MHz	-	11806	-	pF
C _{oss}	Output Capacitance		-	1347	-	
C _{rss}	Reverse Transfer Capacitance		-	66	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} = 60 V, V _{GEN} = 10 V, R _G = 3.9 Ω, R _L = 1.2 Ω, I _{DS} = 50 A	-	31	-	nS
t _r	Turn-on Rise Time		-	109	-	
t _{d(off)}	Turn-off Delay Time		-	150	-	
t _f	Turn-off Fall Time		-	109	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} = 60 V, V _{GS} = 10 V, I _{DS} = 50 A	-	216	-	nC
Q _{gs}	Gate-Source Charge		-	61	-	
Q _{gd}	Gate-Drain Charge		-	56	-	

Notes :

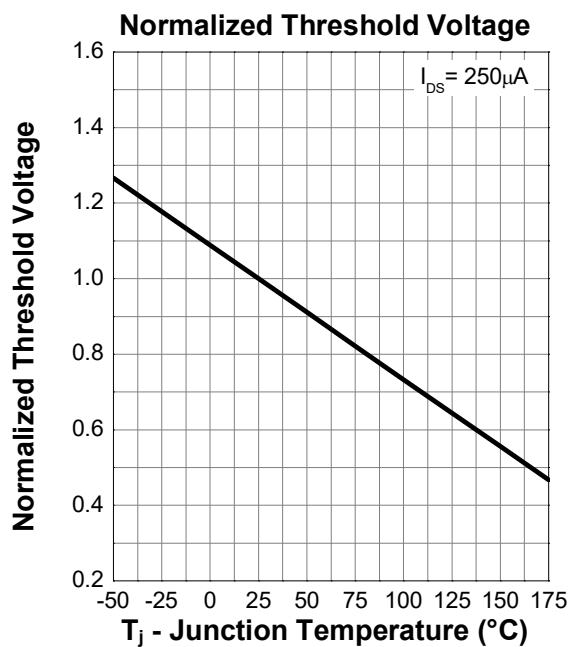
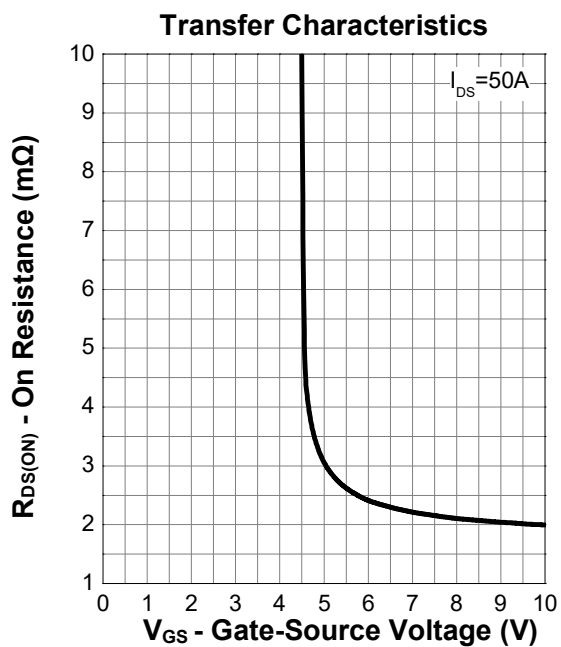
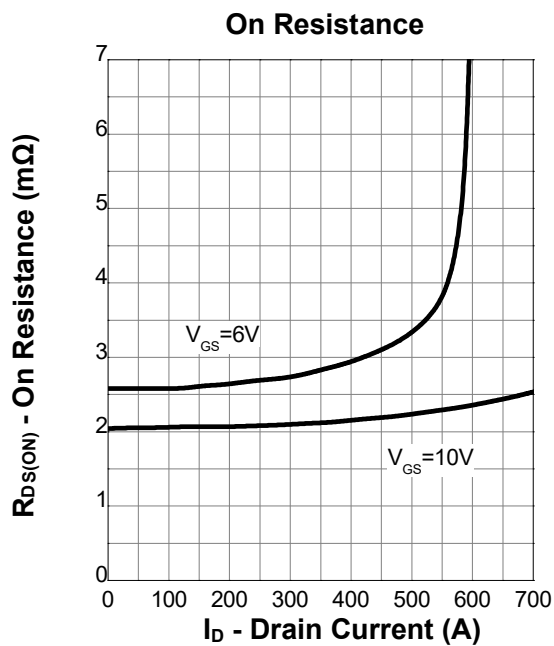
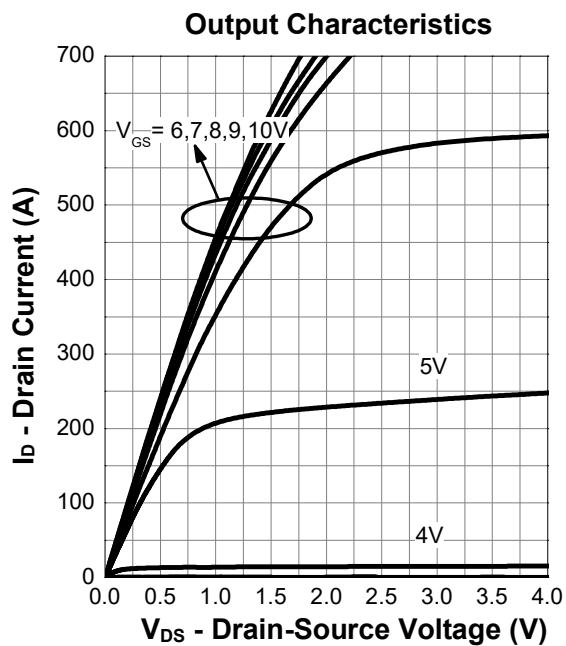
a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

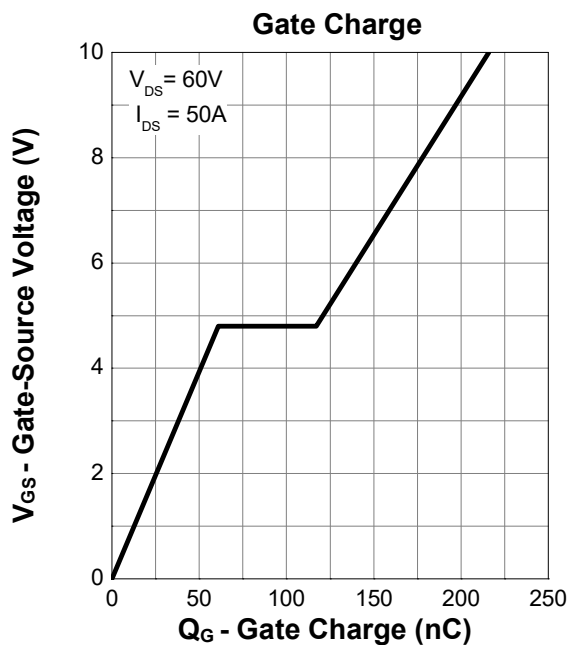
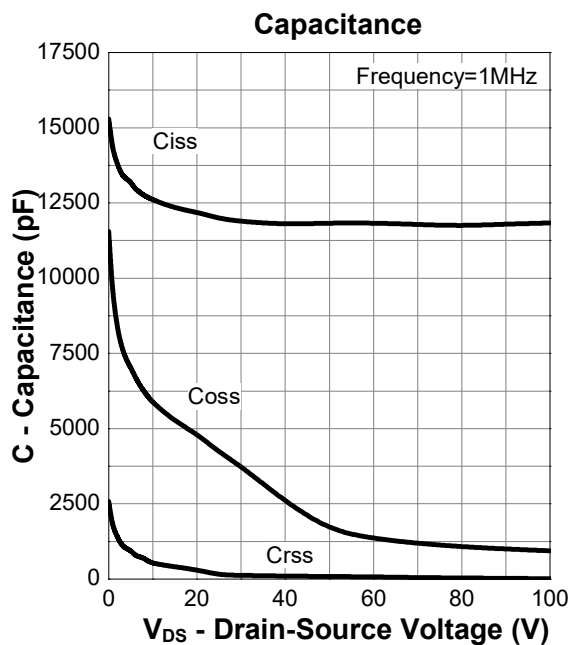
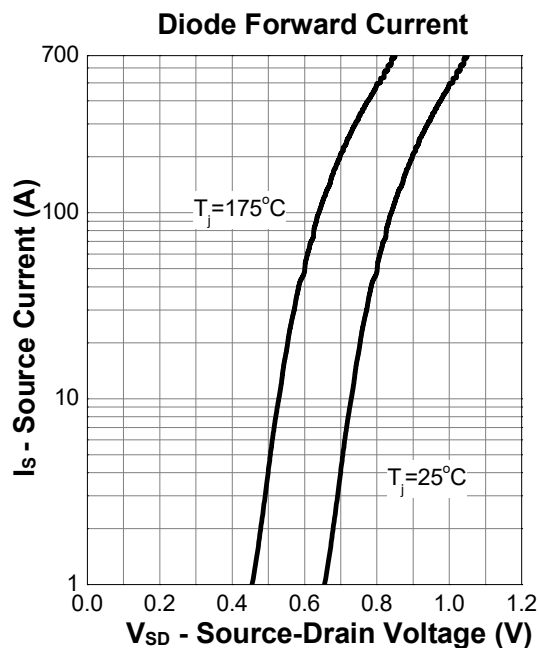
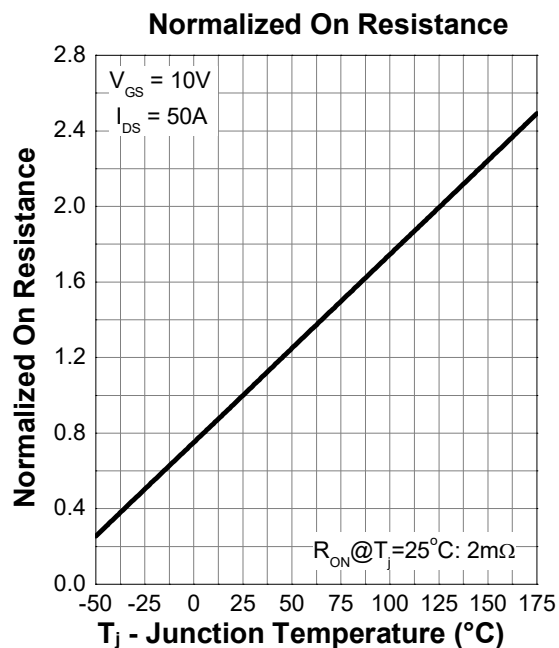
7. Typical Characteristics



7. Typical Characteristics (cont.)

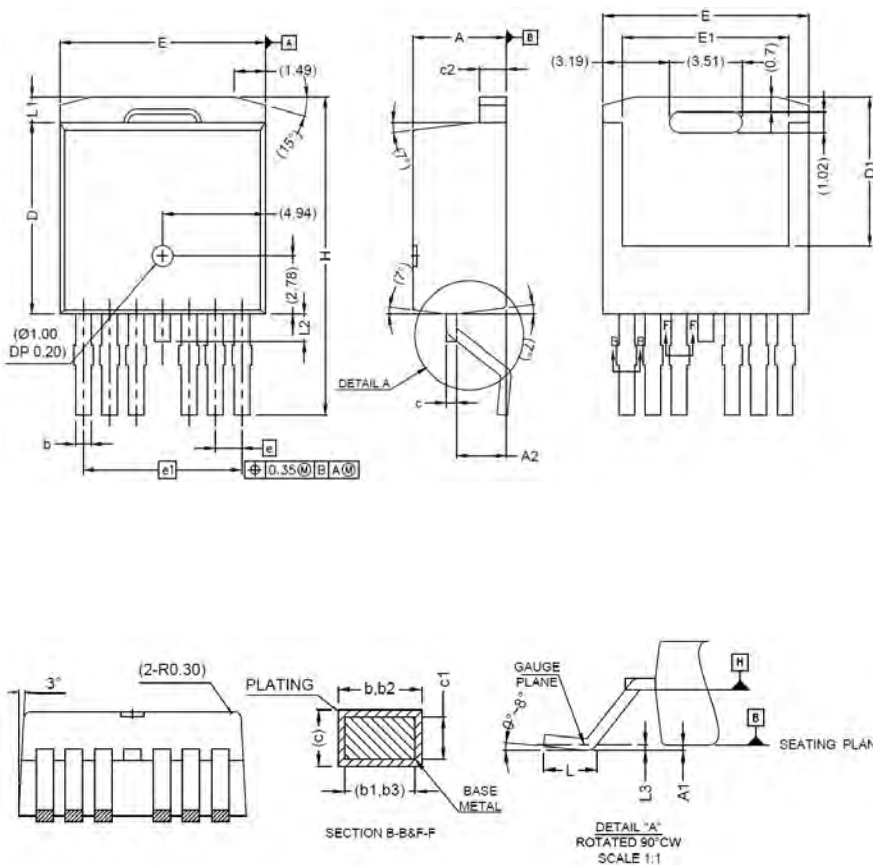


7. Typical Characteristics (cont.)



8. Package Dimensions

TO-263-7L Package



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	4.30	4.70
A1	-	0.25
A2	2.20	2.60
b	0.65	0.85
b1	0.65	0.80
b2	0.80	1.00
b3	0.80	0.95
c	0.45	0.60
c1	0.45	0.55
c2	1.25	1.40
D	9.00	9.40
D1	6.86	7.42
E	9.68	10.08
E1	7.70	8.30
e	1.27 BSC	
e1	7.62 BSC	
L	1.78	2.79
L1	-	1.60
L2	-	1.78
L3	0.25BSD	
H	14.61	15.88