

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☒ Surface-mounted package
- ☒ Advanced trench cell design

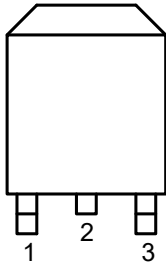
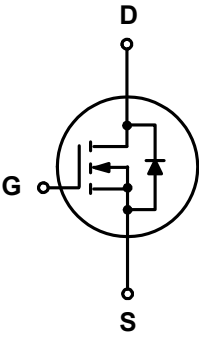
1.2 Applications

- ☒ LCD TV appliances
- ☒ LCDM appliances
- ☒ High power inverter system

1.3 Quick reference

- ☒ $BV \geq 150 \text{ V}$
- ☒ $P_{tot} \leq 50 \text{ W}$
- ☒ $I_D \leq 21 \text{ A}$
- ☒ $R_{DS(ON)} \leq 40\text{m}\Omega @ V_{GS} = 10 \text{ V}$
- ☒ $R_{DS(ON)} \leq 46\text{m}\Omega @ V_{GS} = 6 \text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)	 Top View TO252	
2	Drain(D)		
3	Source(S)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _C = 25 °C	150	-	V
V _{GS}	Gate-Source Voltage	T _C = 25 °C	-	±20	V
I _D	Drain Current (DC)	T _C = 25 °C, V _{GS} = 10 V	-	21	A
		T _C = 100 °C, V _{GS} = 10 V	-	13.8	A
I _{DM} *	Drain Current (Pulsed)	T _C = 25 °C, V _{GS} = 10 V	-	84	A
P _{tot}	Drain power dissipation	T _C = 25 °C	-	50	W
T _{stg}	Storage Temperature		-55	150	°C
T _J	Junction Temperature		-	150	°C
I _S	Continuous-Source Current	T _C = 25 °C	-	21	A
R _{θJA} **	Thermal Resistance- Junction to Ambient		-	37	°C/W
R _{θJC} **	Thermal Resistance- Junction to Case		-	1.2	

Notes :

* Pulse width ≤ 300 μs, duty cycle ≤ 2 %

** Mounted on Large Heat Sink

*** limited by bonding wire

4. Marking Information

Product Name	Marking
UP20N15K	20N15 YWWXXX YWW: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UP20N15K	TO252			2500	

Note: UOE defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

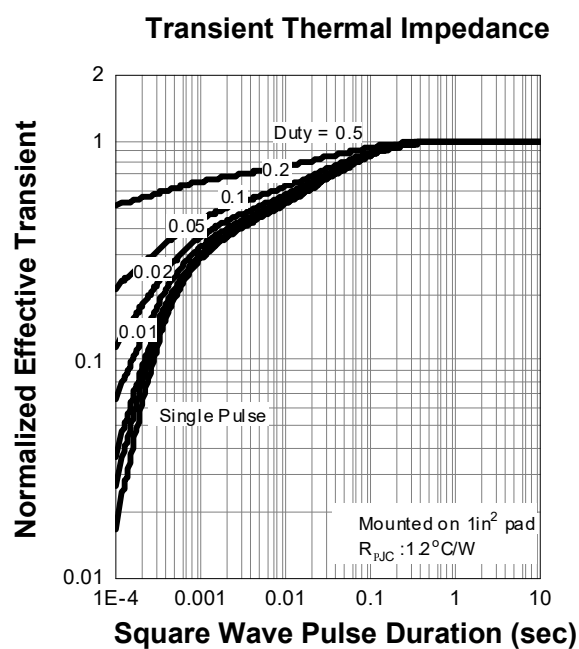
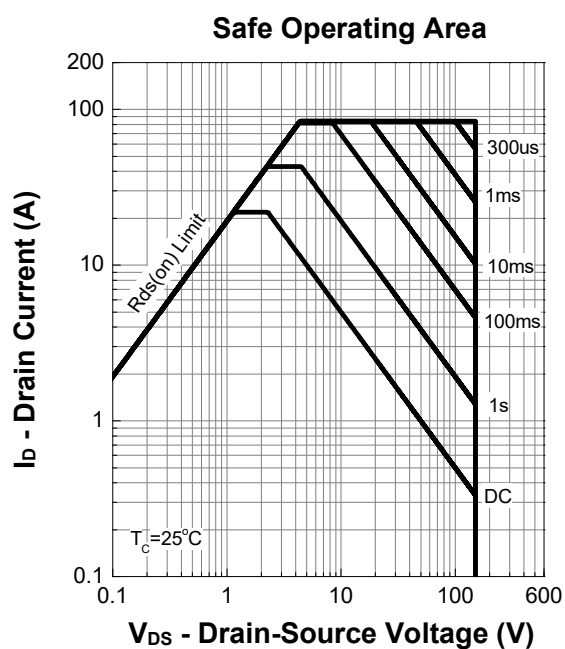
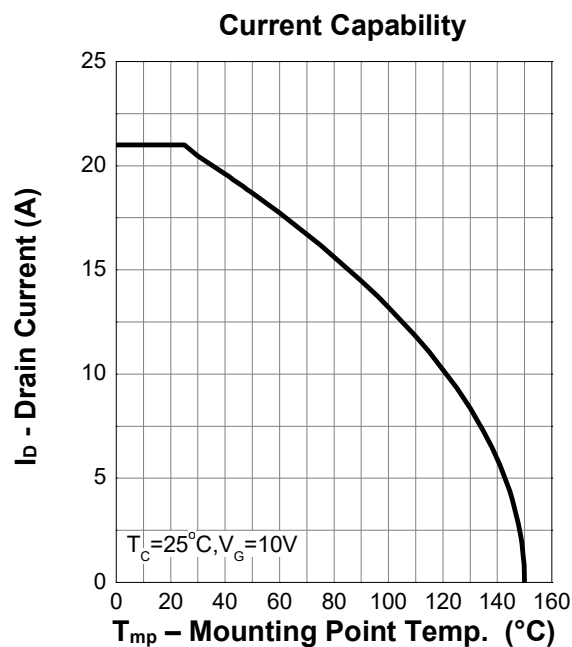
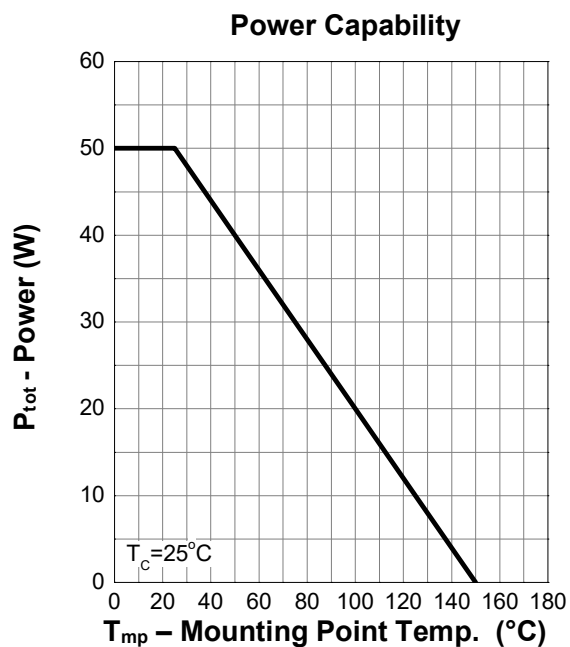
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	150	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	2.0	-	4.0	V
I _{DSS}	Drain Leakage Current	V _{DS} = 120 V, V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} = 0 V, V _{GS} = ± 20 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} = 10 V, I _{DS} = 10 A	-	33	40	m Ω
		V _{GS} = 6 V, I _{DS} =5 A	-	40	46	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 10 A, V _{GS} = 0 V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _{DS} = 4 A, V _{GS} = 0 V dI _{SD} /dt = 100 A/μs	-	72	-	ns
Q _{rr}	Reverse Recovery Charge		-	143	-	μC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 75 V Frequency = 1 MHz	-	1232	-	pF
C _{oss}	Output Capacitance		-	81	-	
C _{rss}	Reverse Transfer Capacitance		-	32	-	
t _{a(on)}	Turn-on Delay Time	V _{DS} = 75 V, V _{GEN} = 10 V, R _G = 4.5 Ω, R _L = 7.5 Ω, I _{DS} = 10 A	-	11	-	ns
t _r	Turn-on Rise Time		-	40	-	
t _{a(off)}	Turn-off Delay Time		-	19	-	
t _f	Turn-off Fall Time		-	32	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} = 75 V, V _{GS} = 10 V, I _{DS} = 10 A	-	25.8	-	nC
Q _{gs}	Gate-Source Charge		-	8	-	
Q _{gd}	Gate-Drain Charge		-	8.3	-	

Notes :

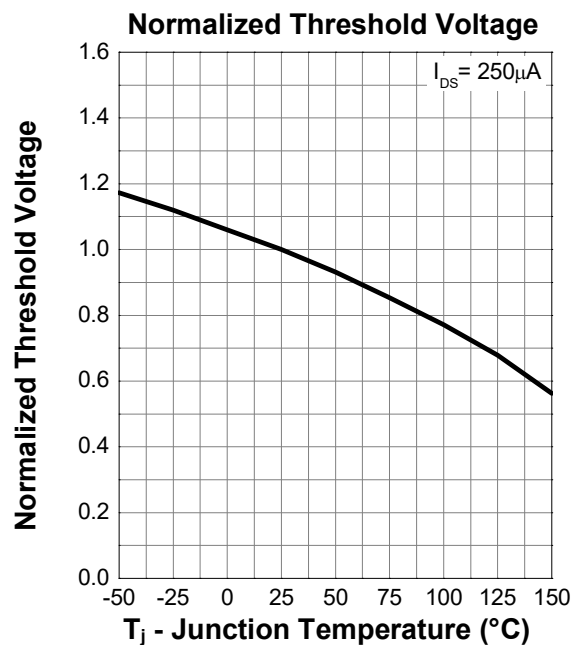
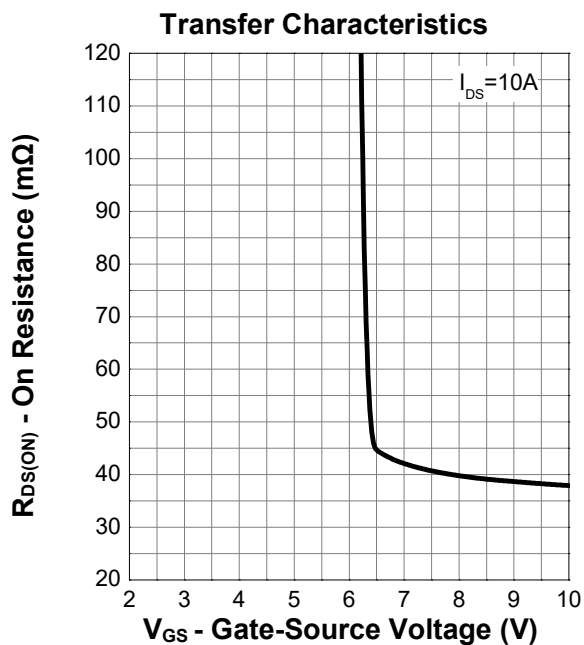
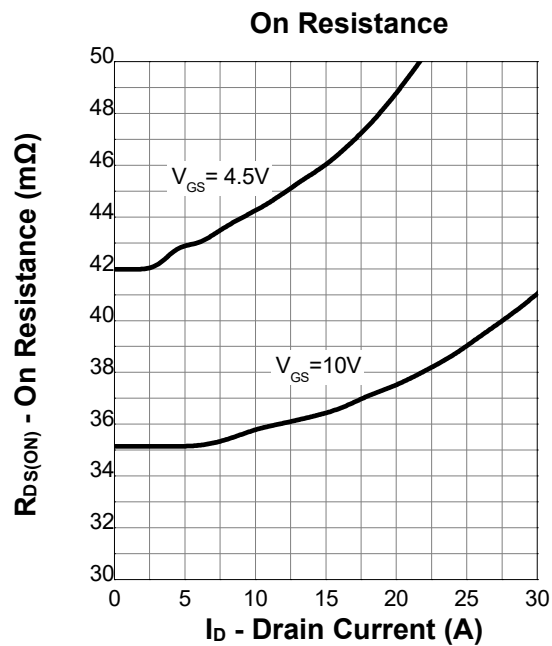
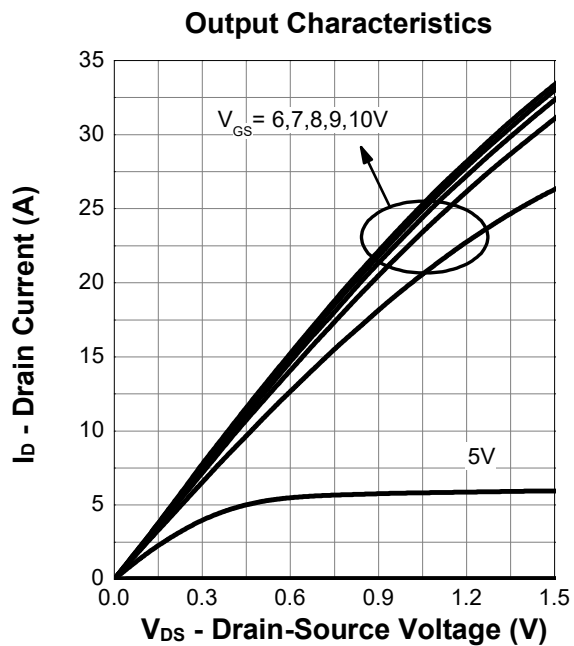
a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

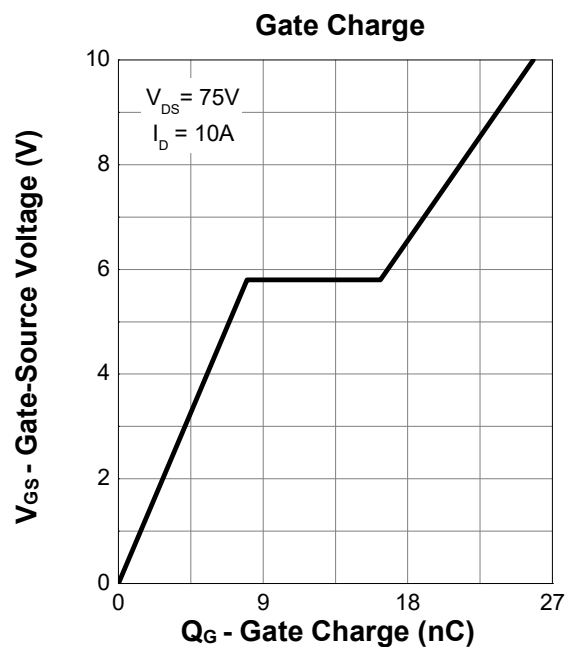
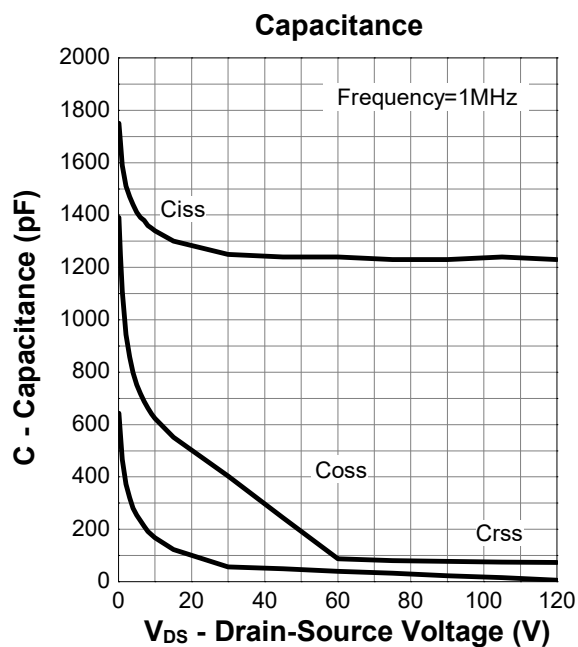
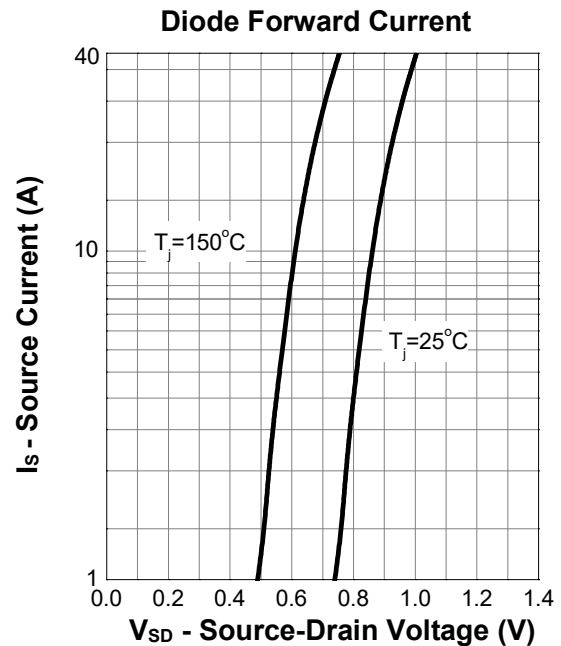
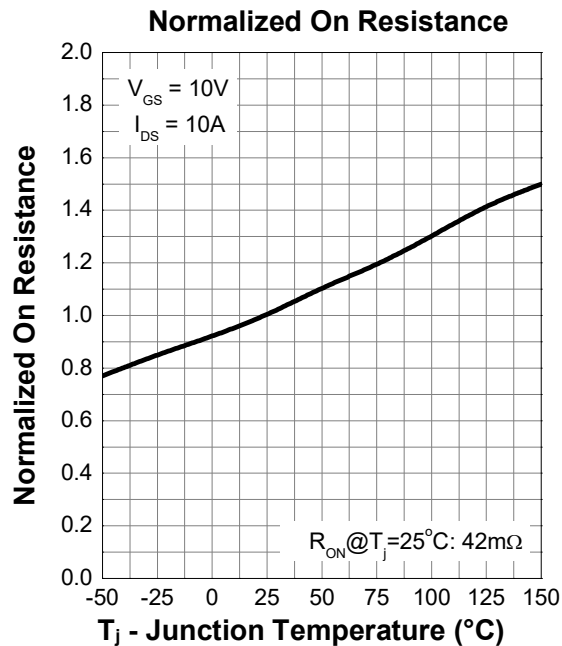
7. Typical Characteristics



7. Typical Characteristics (cont.)

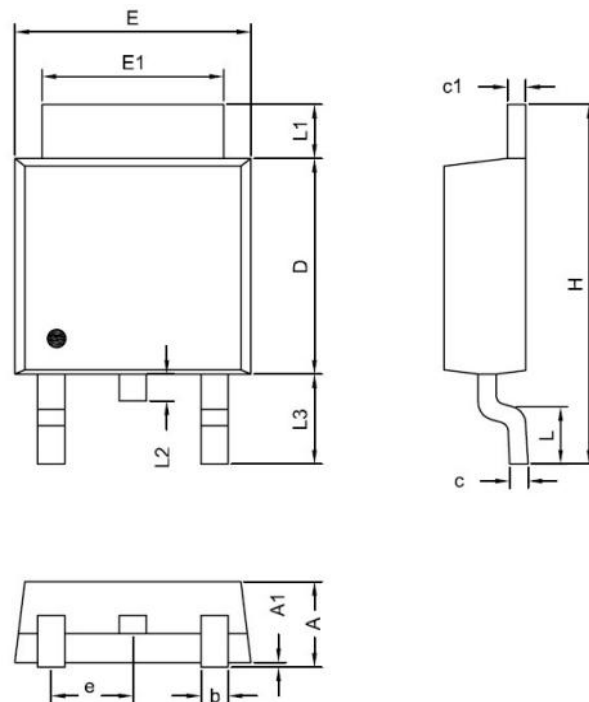


7. Typical Characteristics (cont.)



8.Package Dimensions

TO252-3L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	2.19	2.38
A1	0.02	0.13
D	5.30	6.40
E	6.35	6.80
E1	5.20	5.50
c	0.40	0.60
c1	0.40	0.60
b	0.55	0.85
e	2.30 BCS	
L	1.00	1.80
L1	0.70	1.80
L2	0.70 BCS	
L3	2.40	2.80
H	9.20	10.40