N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Advanced trench cell design

1.2 Applications

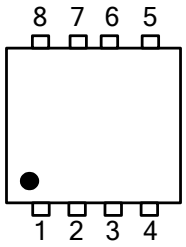
- ☑ MB and NB
- ☑ Half – bridge Drivers
- ☑ Motor drivers

1.3 Quick reference

- ☑ BV ≧ 16 V
- ☑ P_{tot} ≦ 7.8 W
- ☑ I_D ≦ 50 A
- ☑ $R_{DS(ON)}$ ≦ 3.8 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ ≦ 5.5 mΩ @ V_{GS} = 2.5 V

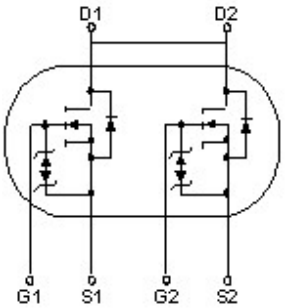
2. Pin Description

Pin	Description
1,2,3	Source(S1)
4	Gate(G1)
5	Gate(G2)
6,7,8	Source(S2)



Top View

PDFN3x3-8L(Dual)



2. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	16	-	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	± 10	V
I_D*	Drain Current (DC)	T_C = 25 ℃, V_{GS} = 10 V	-	50	A
		T_C = 100 ℃, V_{GS} = 10 V	-	21	A
I_{DM}*,**,***	Drain Current (Pulsed)	T_C = 25 ℃, V_{GS} = 10 V	-	92	A
P_{tot}*	Total Power Dissipation	T_C = 25 ℃	-	7.8	W
T_{stg}	Storage Temperature		- 55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Diode Forward Current	T_C = 25 ℃	-	50	A
$R_{\theta JA}$*	Thermal Resistance- Junction to Ambient		-	75	℃ / W
$R_{\theta JC}$*	Thermal Resistance- Junction to Case		-	16	

Notes：

* Surface Mounted on 1 in^2 pad area, t ≤ 10 sec

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

*** Limited by bonding wire

4. Marking Information

Product Name	Marking
UD3325Q	3325 YWWXXX YWW: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UD3325Q	DFN3*3			3000	

6. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	16	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.5	-	1.0	V
I_{DSS}	Zero Gate Voltage Source Current	V_{DS} = 10 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 10 V, V_{DS} = 0 V	-	-	± 10	μA
$R_{DS(ON)}$[a]	Drain-Source On-State Resistance	V_{GS} = 4.5 V, I_D = 20A	-	3.3	3.8	mΩ
		V_{GS} = 2.5 V, I_D = 10A	-	4.5	5.5	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 20 A, V_{GS} = 0 V	-	-	1.2	V
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 6 V Frequency = 1 MHz	-	2468	-	pF
C_{oss}	Output Capacitance		-	580	-	
C_{rss}	Reverse Transfer Capacitance		-	528	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 6 V, V_{GEN} = 4.5 V, R_G = 4.5 Ω, R_L = 0.3Ω, I_D = 20 A	-	0.9	-	uS
t_r	Turn-on Rise Time		-	2	-	
t_d(off)	Turn-off Delay Time		-	3.3	-	
t_f	Turn-off Fall Time		-	5.7	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 6 V, I_{DS} = 20 A	-	40	-	nC
Q_{gs}	Gate-Source Charge		-	4.5	-	
Q_{gd}	Gate-Drain Charge		-	6.9	-	

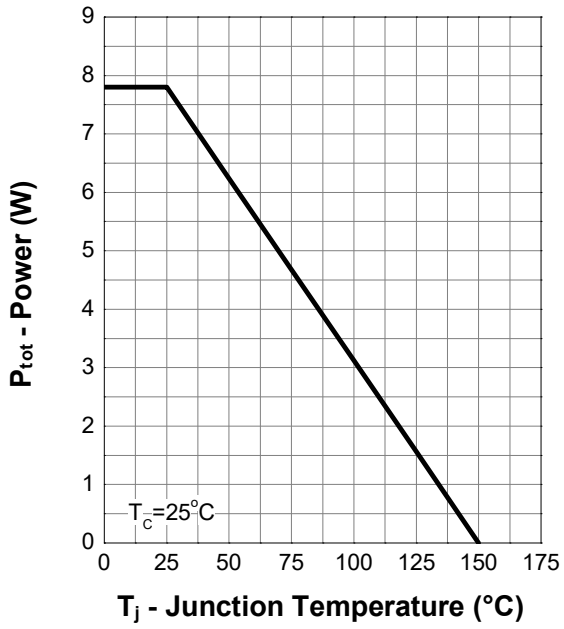
Notes：

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2 %

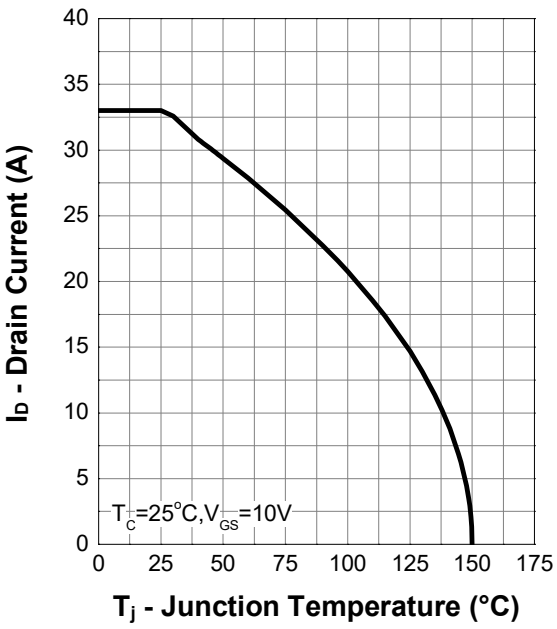
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics (Cont.)

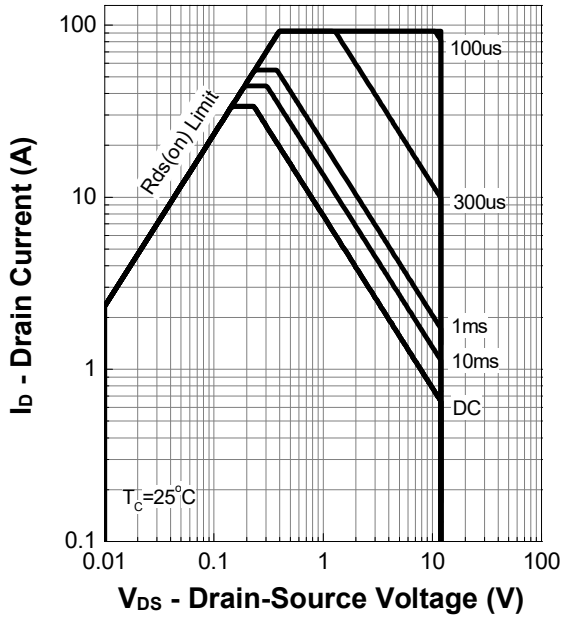
Power Capability



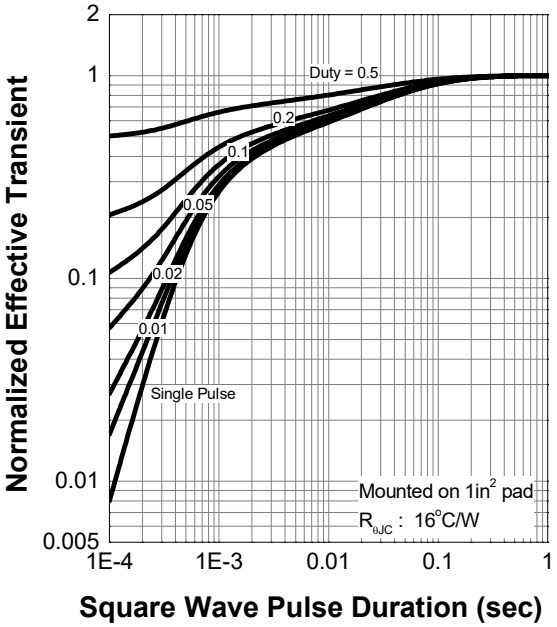
Current Capability



Safe Operation Area

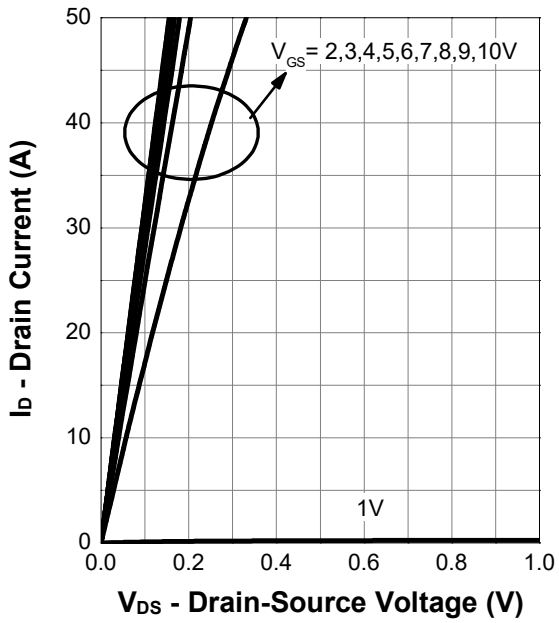


Transient Thermal Impedance

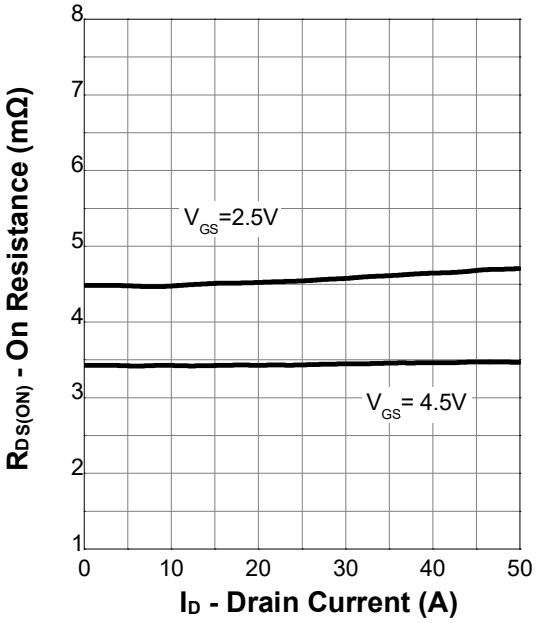


7. Typical Characteristics (Cont.)

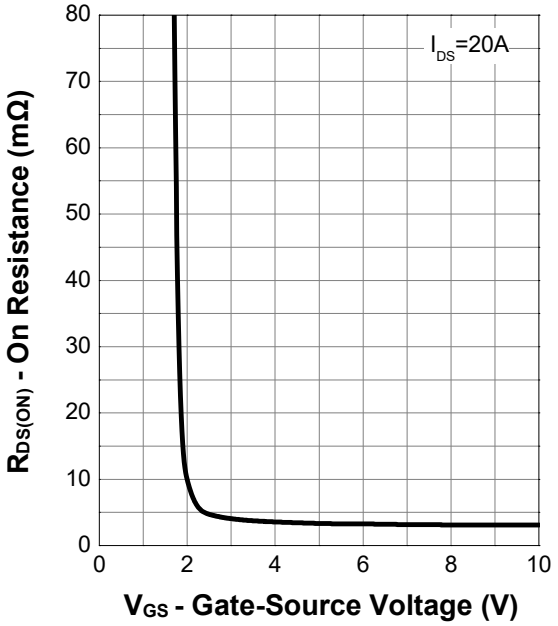
Output Characteristics



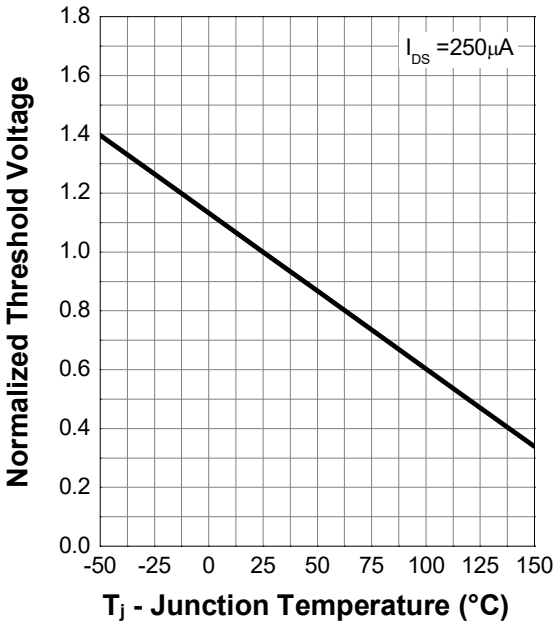
On Resistance



Transfer Characteristics

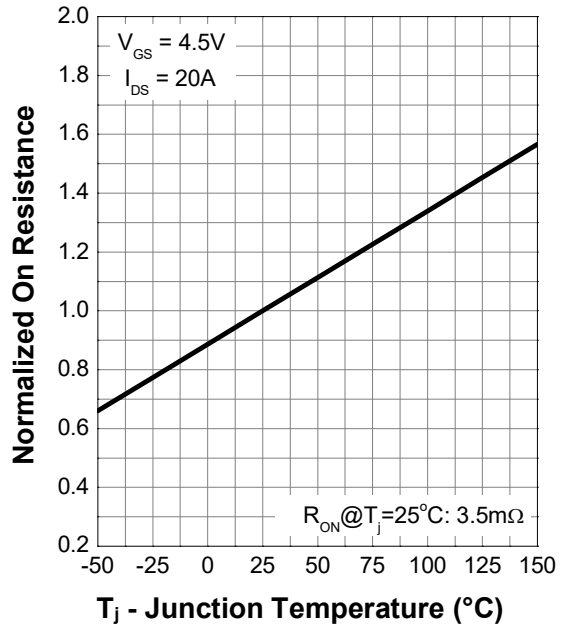


Normalized Threshold Voltage

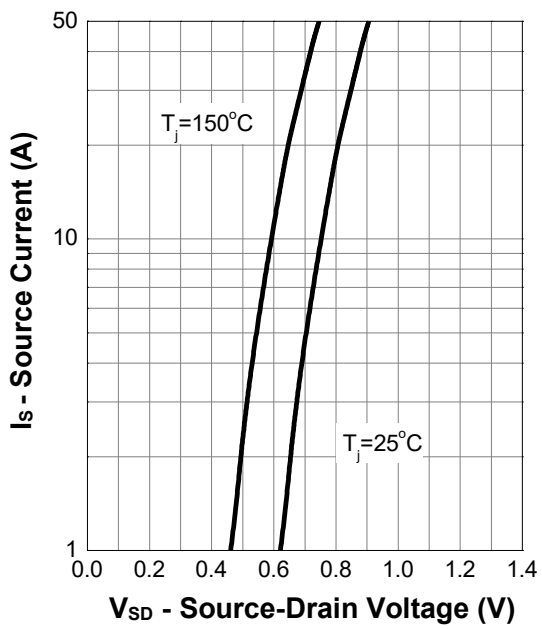


7. Typical Characteristics (Cont.)

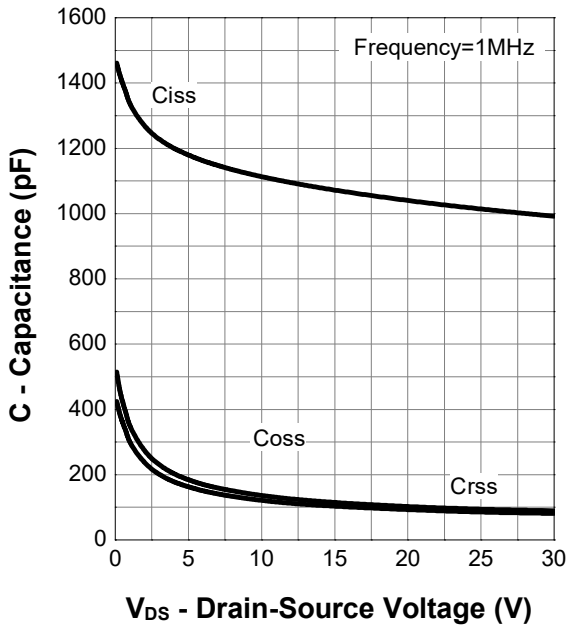
Normalized On Resistance



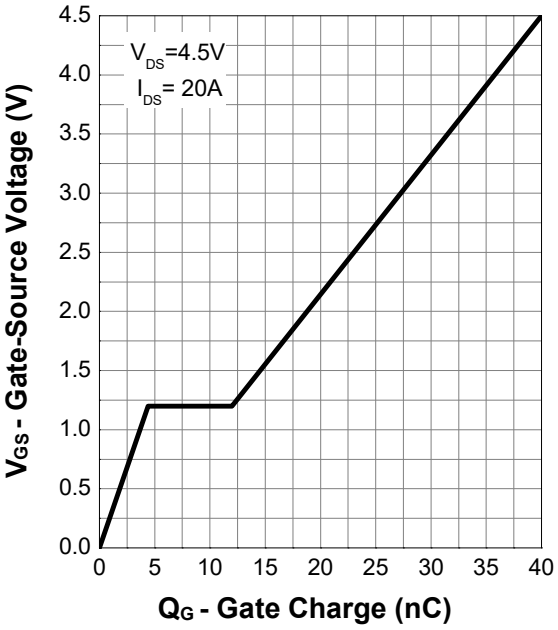
Diode Forward Current



Capacitance

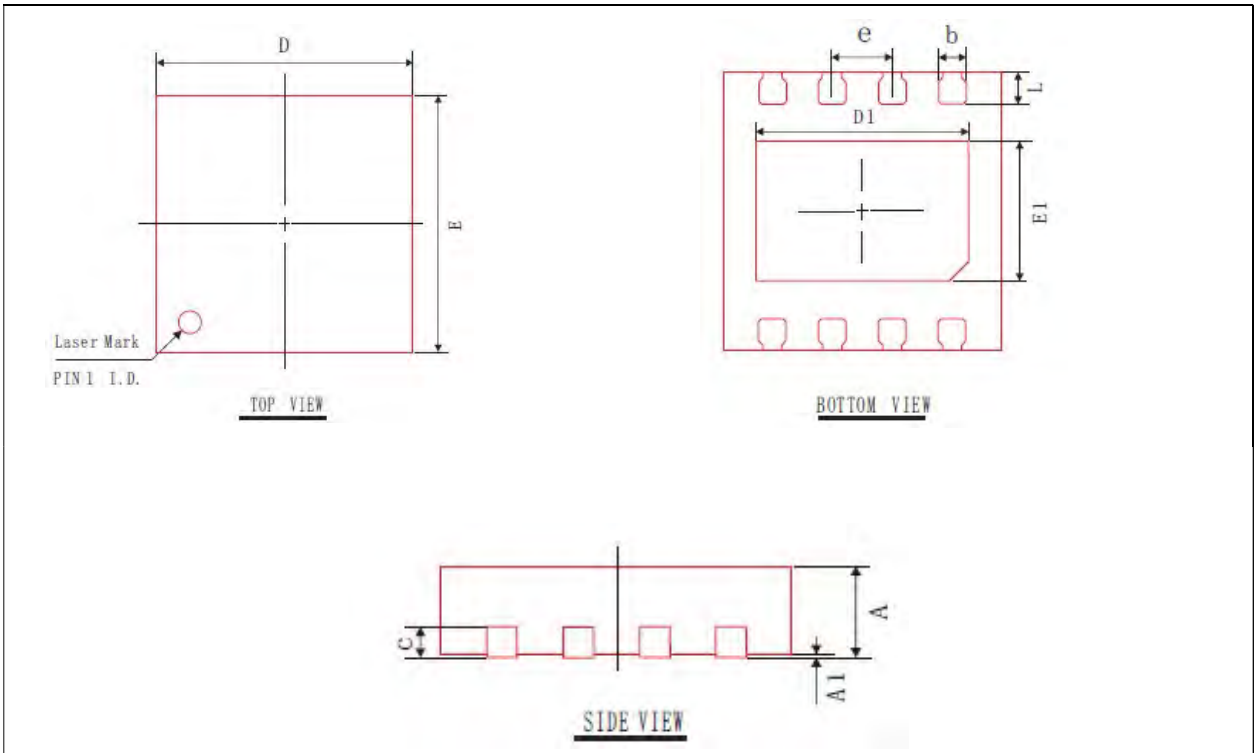


Gate Charge



8. Package Dimensions

DFN3x3 - 8L Package



PKG	DFN3*3-8L		
SYMBOL	MIN	TYP	MAX
A	0.70	O.75	0.80
A1	0.00	0.02	0.05
c		0.203REF	
D	2.95	3.00	3.07
E	2.95	3.00	3.07
D1	2.25	2.30	2.35
E1	1.40	1.50	1.60
L	0.25	0.35	0.45
e		0.65BSC	