Dual N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ ESD 2KV
- ☑ Advanced trench cell design

1.2 Applications

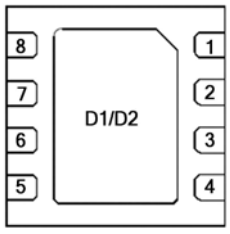
- ☑ Motor application
- ☑ High power inverter system

1.3 Quick reference

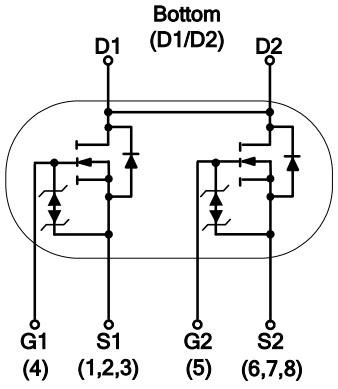
- ☑ BV ≧ 20 V
- ☑ P_{tot} ≦ 31 W
- ☑ I_D ≦ 49 A
- ☑ $R_{DS(ON)}$ ≦ 7.0 mΩ @ V_{GS} = 4.5 V
- ☑ $R_{DS(ON)}$ ≦ 8.0 mΩ @ V_{GS} = 3.9 V
- ☑ $R_{DS(ON)}$ ≦ 9.5 mΩ @ V_{GS} = 2.5 V

2. Pin Description

Pin	Description
1,2,3	Source(S1)
4	Gate(G1)
5	Gate (G2)
6,7,8	Source (S2)



Bottom View
DFN3X3-8L



3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	20	-	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	± 10	V
I_D*,***	Drain Current	T_C = 25 ℃, V_{GS} = 10 V	-	49	A
I_{DM}*,***	Pulsed Drain Current	T_C = 25 ℃, V_{GS} = 10 V	-	99	A
P_{tot}	Total Power Dissipation	T_C = 25 ℃	-	31	W
T_{stg}	Storage Temperature		- 55	150	℃
T_J	Junction Temperature		- 55	150	℃
I_S	Diode Forward Current	T_C = 25 ℃	-	49	A
$R_{\theta JC}$*	Thermal Resistance- Junction to Ambient		-	16	℃ / W

Notes：

* Surface Mounted on 1 in^2 pad area, t ≤ 10 sec

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

*** limited by bonding wire

4. Marking Information

Product Name	Marking
UD3380Q	3380 YWWXXX YWWXXX: Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UD3380Q	DFN3*3			3000	

Note: UOE defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics (T_A=25 °C Unless Otherwise Noted)

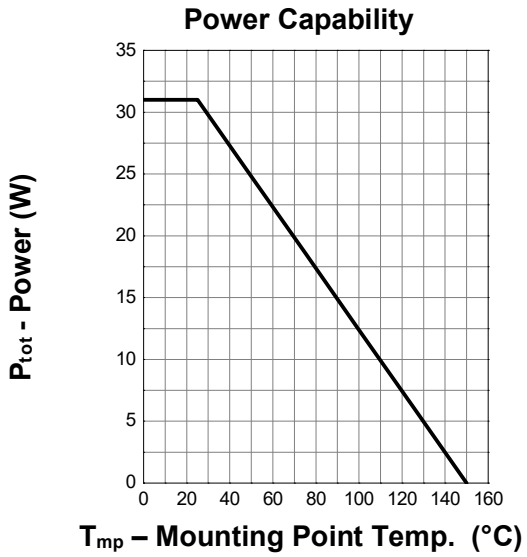
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	20	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.5	-	1.0	V
I_{DSS}	Drain Leakage Current	V_{DS} = 16V, V_{GS} = 0 V	-	-	1	μA
		T_J = 85 ℃	-	-	30	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ±10 V, V_{DS} = 0 V	-	-	± 10	μA
$R_{DS(ON)}$[a]	On-State Resistance	V_{GS} = 4.5 V, I_{DS} = 10 A	-	6.5	7.0	mΩ
		V_{GS} = 3.9 V, I_{DS} = 8 A	-	7.0	8.0	
		V_{GS} = 2.5 V, I_{DS} = 6 A	-	8.2	9.5	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 10 A, V_{GS} = 0V	-	-	1.2	V
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 10 V Frequency = 1MHz	-	1370	-	pF
C_{oss}	Output Capacitance		-	186	-	
C_{rss}	Reverse Transfer Capacitance		-	169	-	
t_{d}(on)	Turn-on Delay Time	V_{DS} = 10 V, V_{GEN} = 4.5 V, R_G = 4.5 Ω, R_L =1 Ω, I_{DS} = 10 A	-	226	-	nS
t_r	Turn-on Rise Time		-	487	-	
t_{d}(off)	Turn-off Delay Time		-	2534	-	
t_f	Turn-off Fall Time		-	5084	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 10 V, I_{DS} = 10 A	-	20.6	-	nC
Q_{gs}	Gate-Source Charge		-	2.4	-	
Q_{gd}	Gate-Drain Charge		-	5.2	-	

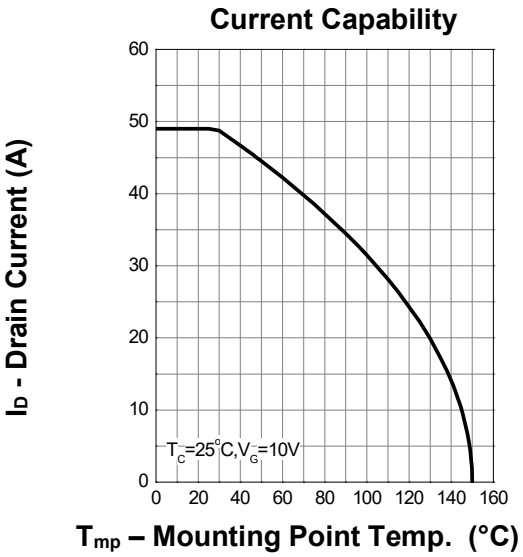
Notes：

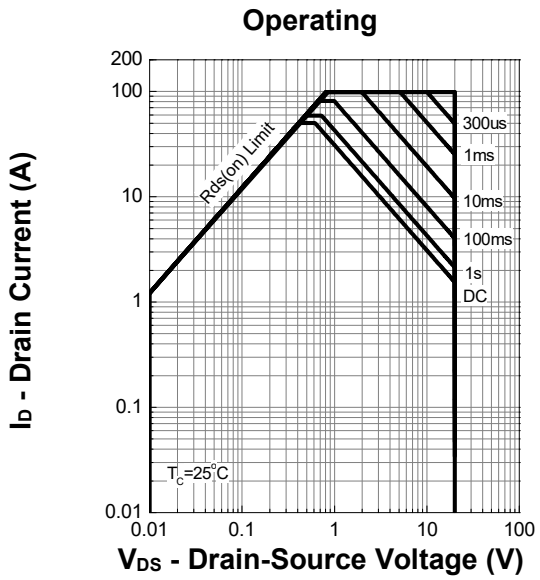
a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%

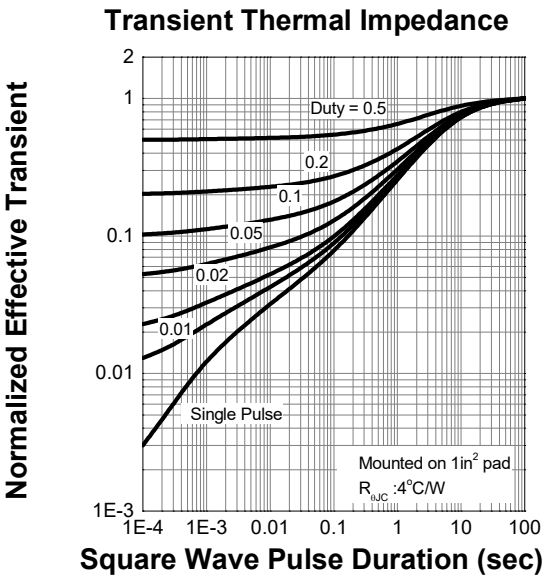
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics



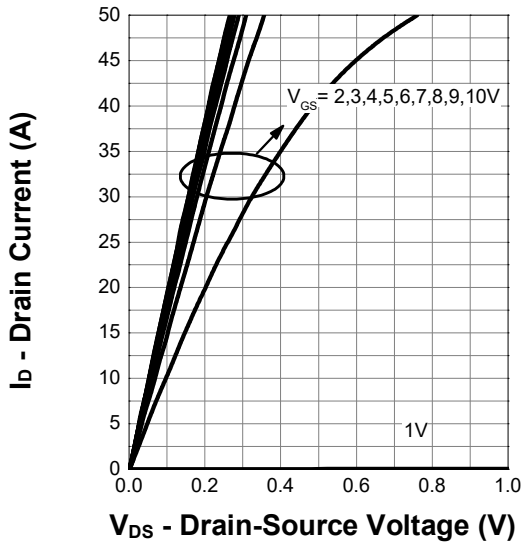




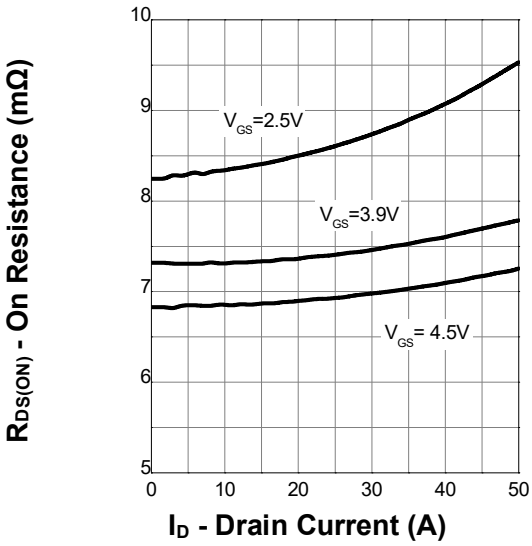


7. Typical Characteristics (cont.)

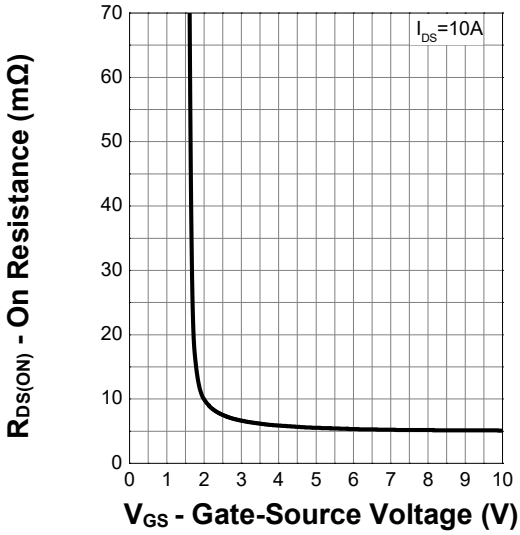
Output Characteristics



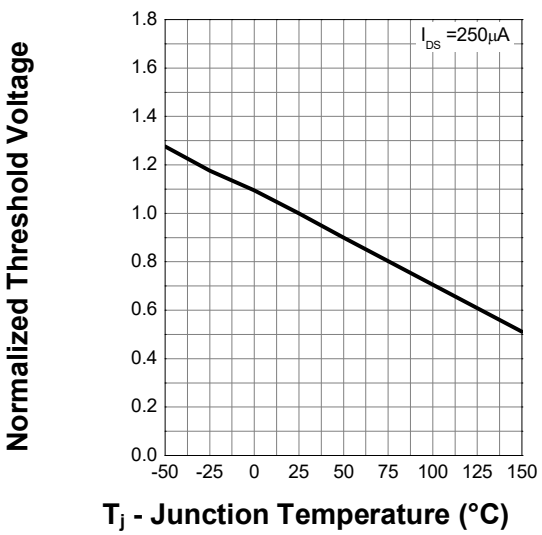
On Resistance



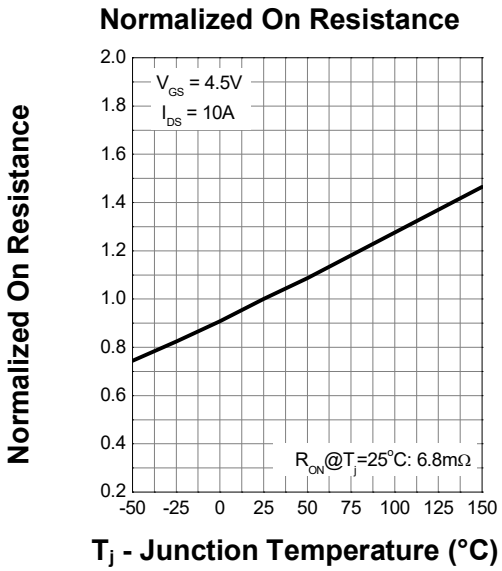
Transfer Characteristics

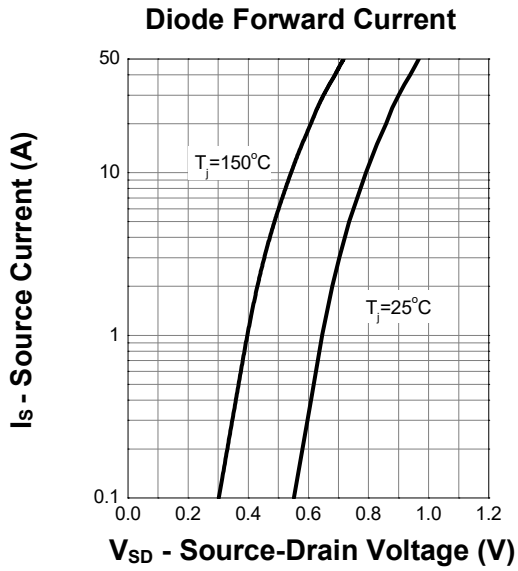


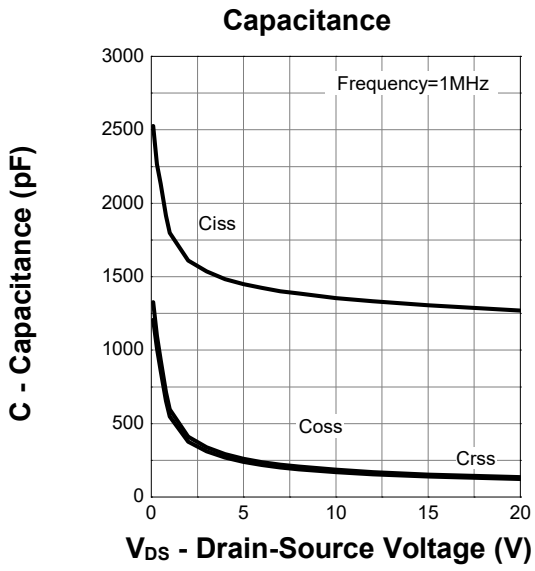
Normalized Threshold Voltage

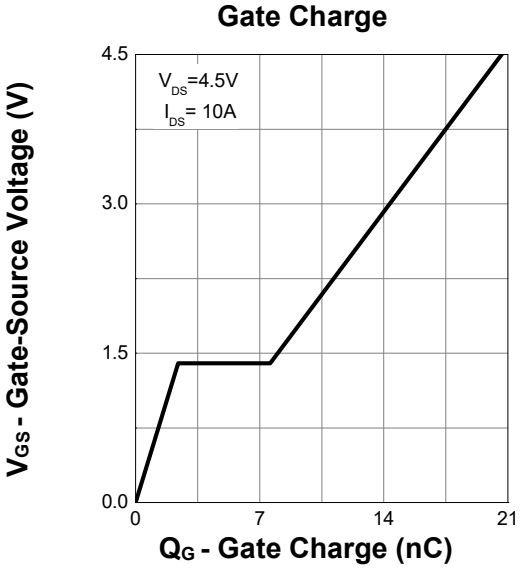


7. Typical Characteristics (cont.)



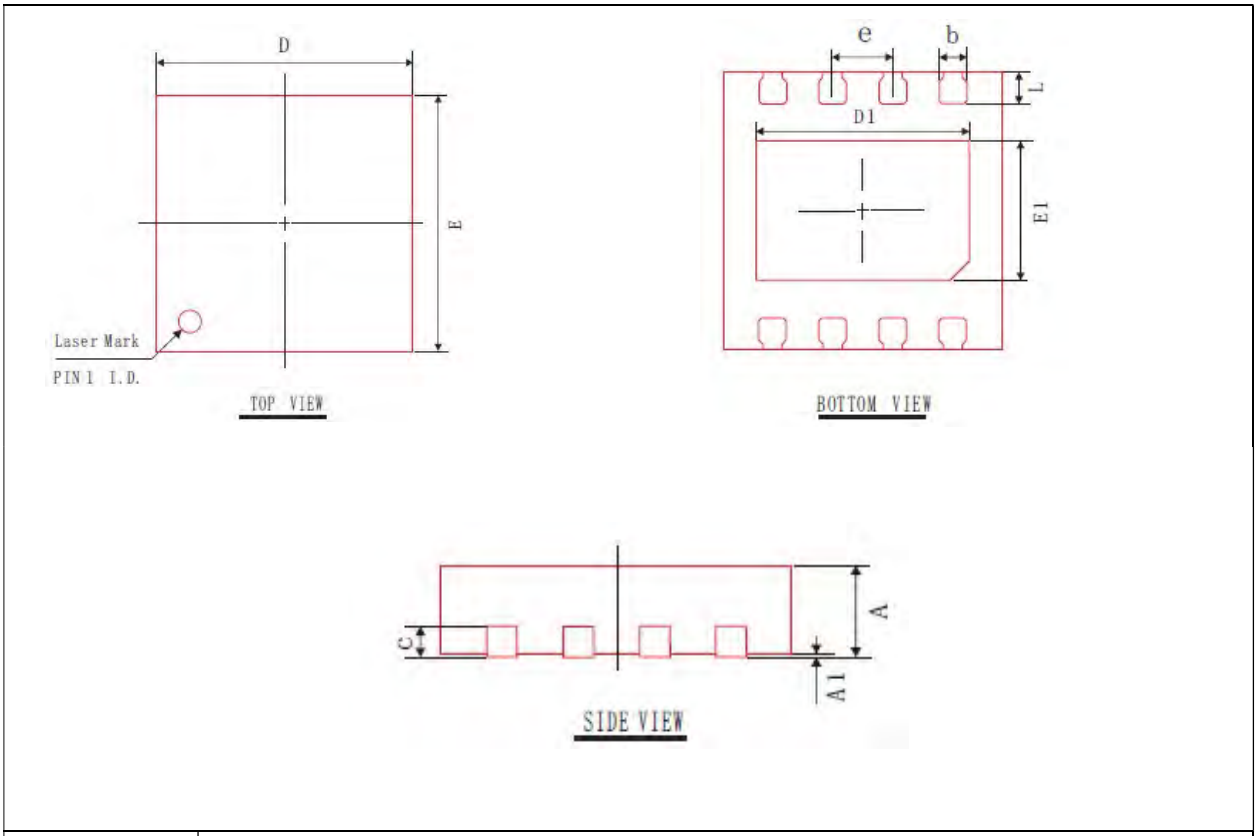






8. Package Dimensions

DFN3x3 - 8L Package



PKG	DFN3*3-8L		
SYMBOL	MIN	TYP	MAX
A	0.70	O.75	0.80
A1	0.00	0.02	0.05
c		0.203REF	
D	2.95	3.00	3.07
E	2.95	3.00	3.07
D1	2.25	2.30	2.35
E1	1.40	1.50	1.60
L	0.25	0.35	0.45
e		0.65BSC	