Dual N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ Advanced trench cell design

1.2 Applications

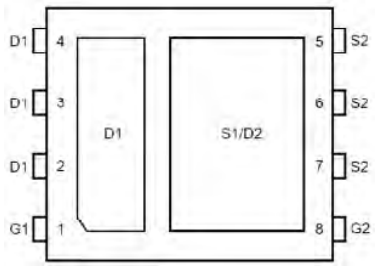
- ☑ LCD TV appliances
- ☑ LCDM appliances
- ☑ High power inverter system

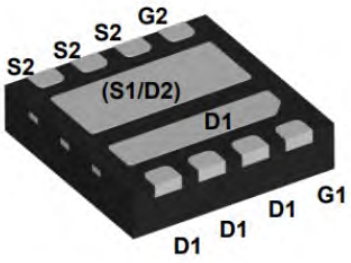
1.3 Quick reference

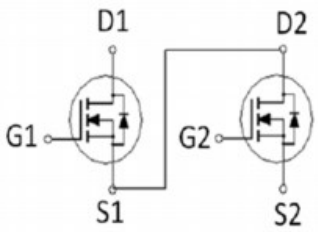
- ☑ BV ≧ 20 V
- ☑ P_{tot} ≦ 50 W
- ☑ I_D ≦ 35 A
- ☑ $R_{DS(ON)}$ ≦ 5.5 mΩ @ V_{GS} = 4.5 V
- ☑ $R_{DS(ON)}$ ≦ 7.8 mΩ @ V_{GS} = 2.5 V

2. Pin Description

Pin	Description	Simplified Outline	Symbol







DFN3x3

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	-	20	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	±10	V
I_D***	Drain Current (DC)	T_C = 25 ℃, V_{GS} = 10 V	-	35	A
		T_C = 100 ℃, V_{GS} = 10 V	-	12	A
I_{DM}*,***	Drain Current (Pulsed)	T_C = 25 ℃, V_{GS} = 10 V	-	35	A
P_{tot}	Drain power dissipation	T_C = 25 ℃	-	50	W
T_{stg}	Storage Temperature		-55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Continuous-Source Current	T_C = 25 ℃	-	35	A
$R_{\theta JA}$**	Thermal Resistance- Junction to Ambient		-	50	℃/W
$R_{\theta JC}$**	Thermal Resistance- Junction to Case		-	2.5	

Notes：
* Pulse width ≤ 300 μs, duty cycle ≤ 2 %
** Mounted on Large Heat Sink
*** limited by bonding wire

4. Marking Information

Product Name	Marking
UD2050CQ	2050 YWWXXX YWWXXX : Date Code

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UD2050CQ	DFN3*3			5000	

6. Electrical Characteristics (T_A=25 ° Unless Otherwise Noted)

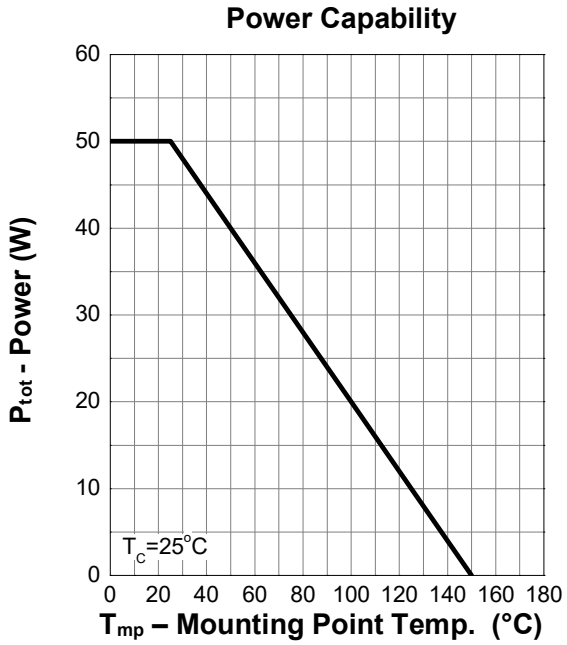
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	20	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.5	-	1.0	V
I_{DSS}	Drain Leakage Current	V_{DS} = 16 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{GS} = 0 V, V_{GS} = ± 10 V	-	-	±10	uA
$R_{DS(ON)}$[a]	On-State Resistance	V_{GS} = 4.5 V, I_{DS} = 20 A	-	5.1	5.5	mΩ
		V_{GS} = 2.5 V, I_{DS} =10 A	-	7.1	7.8	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 20 A, V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_{DS} = 20 A, V_{GS} = 0 V dI_{SD}/dt = 100 A/μs	-	23.8	-	nS
Q_{rr}	Reverse Recovery Charge		-	7	-	nC
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 10 V Frequency = 1 MHz	-	1193	-	pF
C_{oss}	Output Capacitance		-	186	-	
C_{rss}	Reverse Transfer Capacitance		-	174	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 10 V, V_{GEN} = 4.5 V, R_G = 4.5 Ω, R_L = 0.5 Ω, I_{DS} = 20 A	-	12.6	-	nS
t_r	Turn-on Rise Time		-	99.8	-	
t_d(off)	Turn-off Delay Time		-	39.6	-	
t_f	Turn-off Fall Time		-	96.8	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{DS} = 20 A	-	16	-	nC
Q_{gs}	Gate-Source Charge		-	3.7	-	
Q_{gd}	Gate-Drain Charge		-	5.6	-	

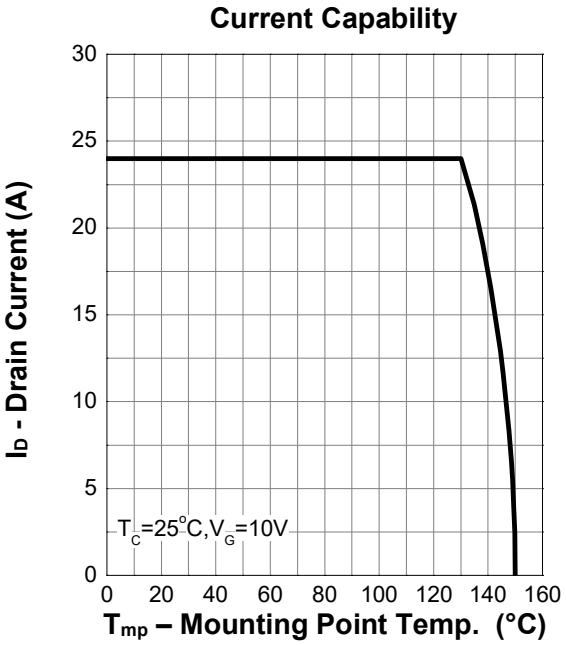
Notes：

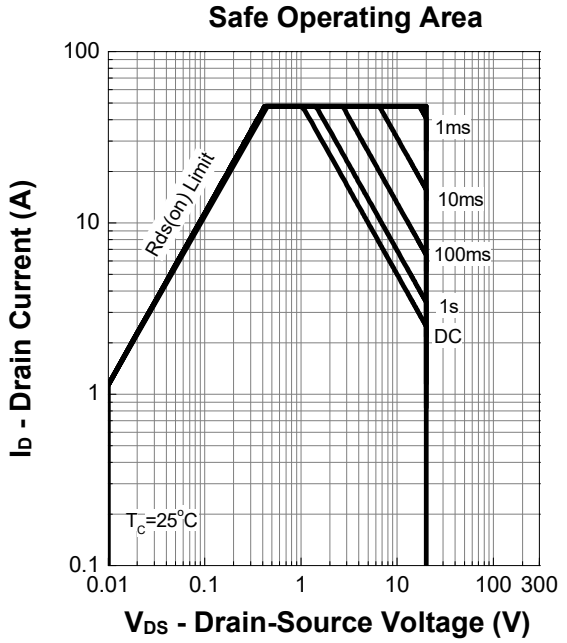
a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%

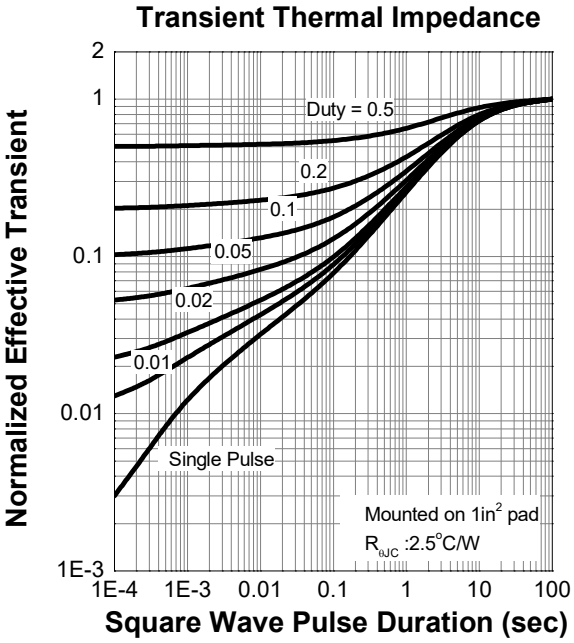
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

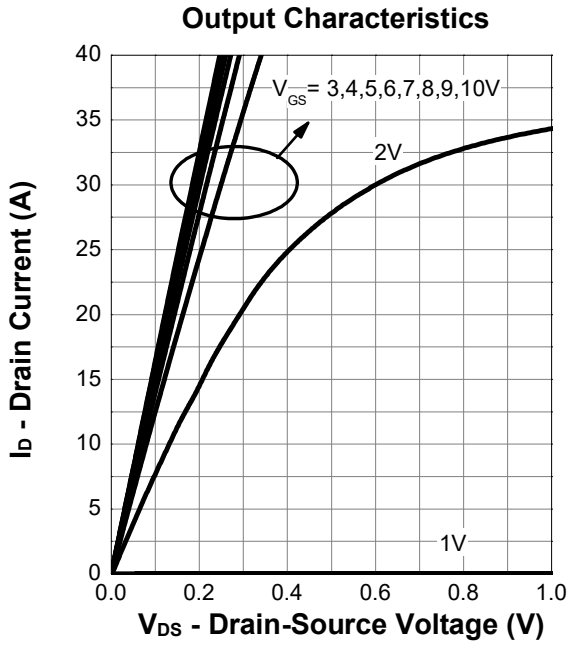


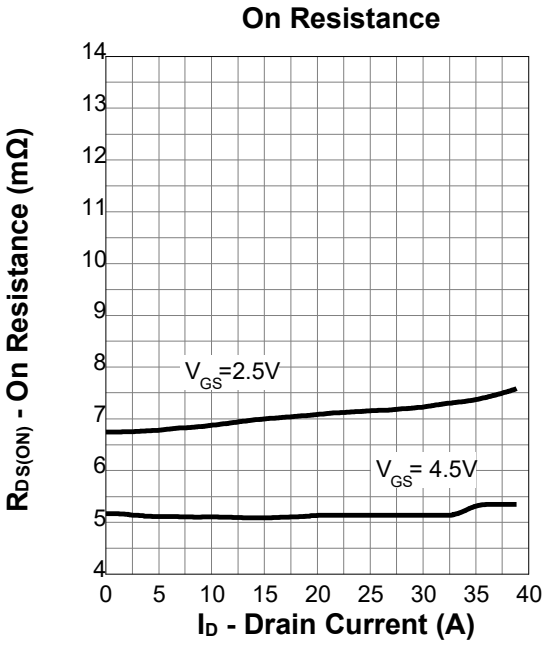


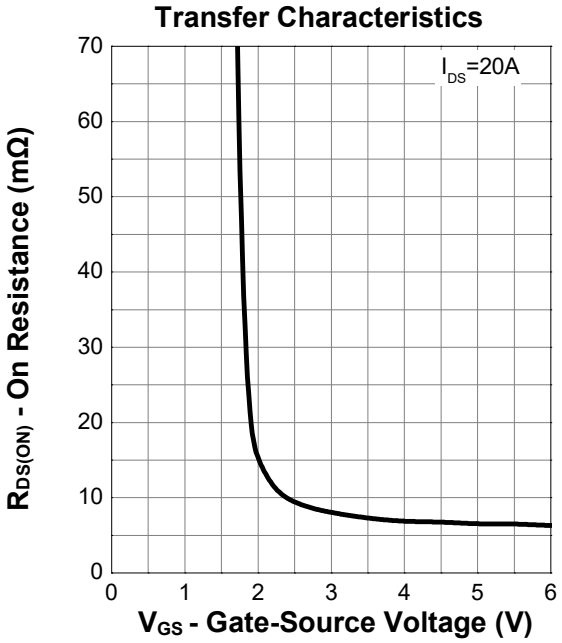


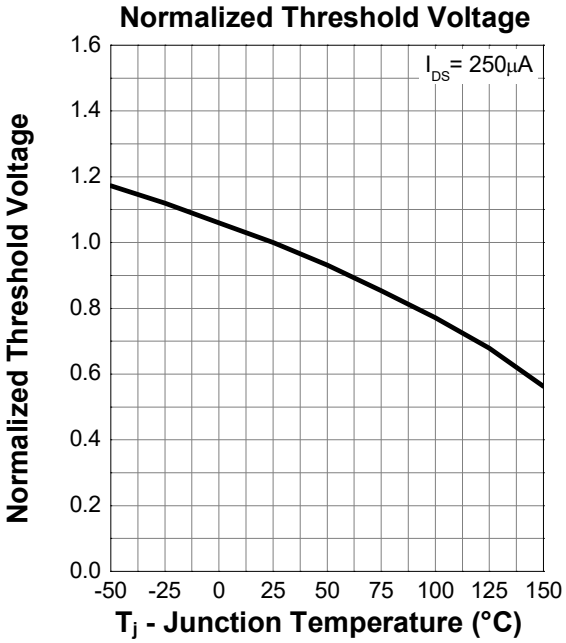


7. Typical Characteristics (cont.)

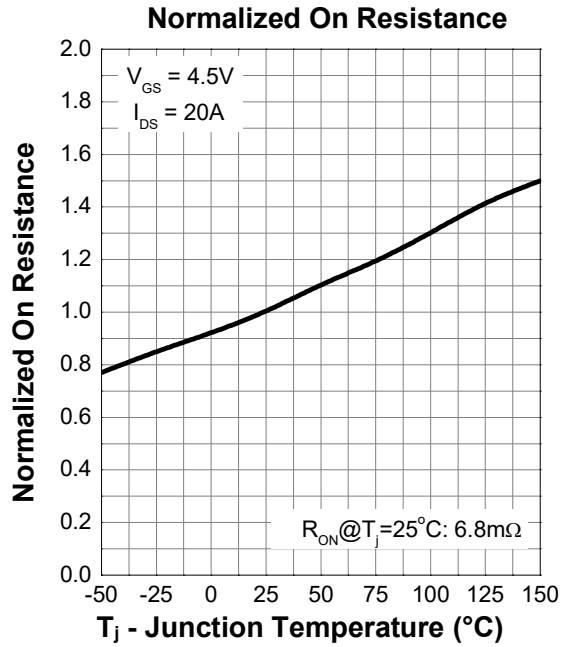


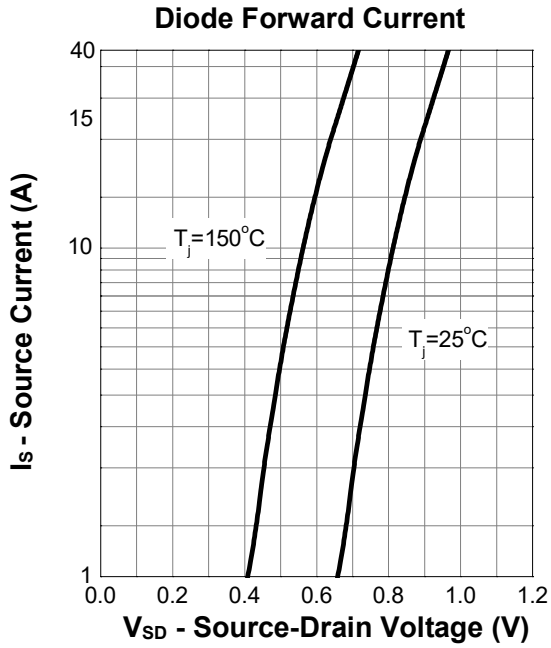


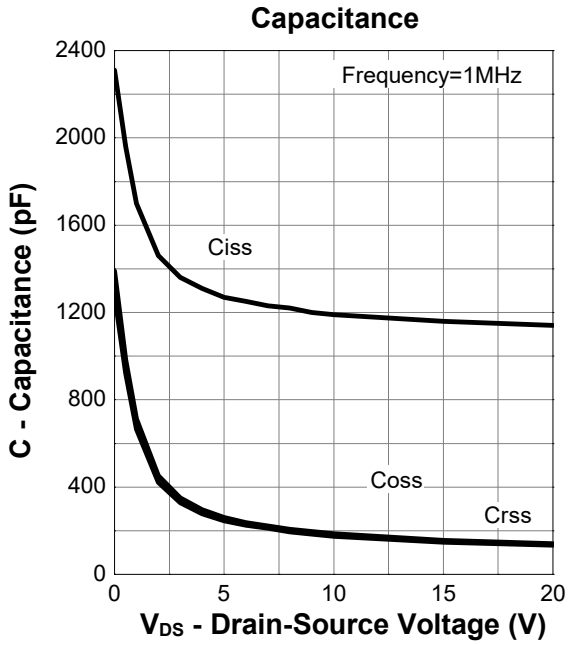


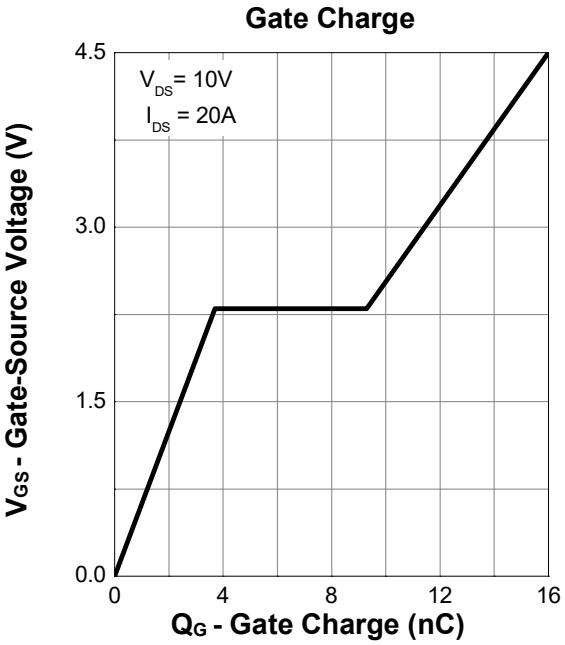


7. Typical Characteristics (cont.)



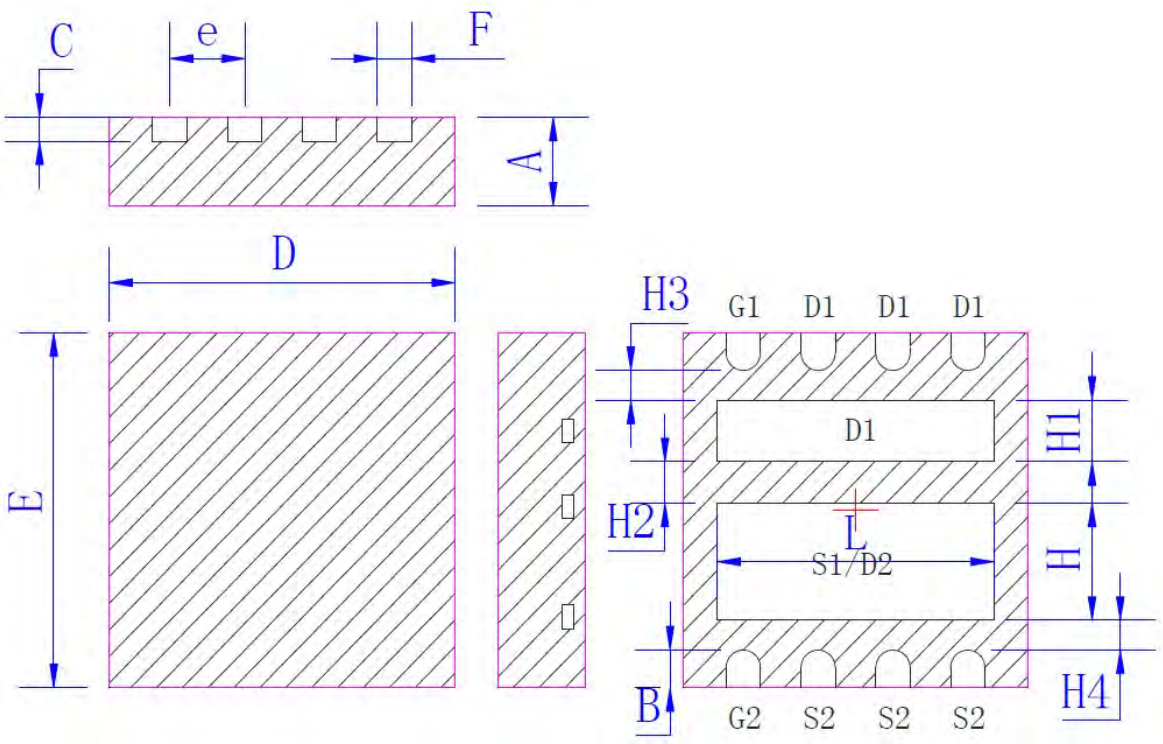






8. Package Dimensions

DFN3*3



Symbol	Min	Typ	Max
A	0.70	0.75	0.80
B	0.27	0.32	0.37
C	0.153	0.203	0.253
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.60	0.65	0.70
F	0.25	0.30	0.35
H	0.89	0.99	1.09
H1	0.42	0.52	0.62
H2	0.25	0.35	0.45
H3	0.15	0.25	0.35
H4	0.15	0.25	0.35
L	2.30	2.40	2.50