

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- Surface-mounted package
- Advanced trench cell design

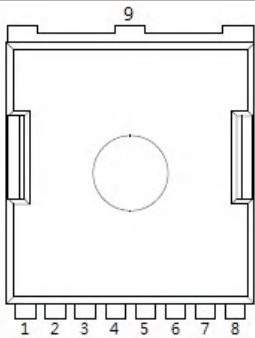
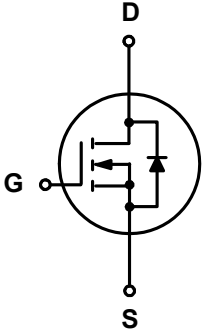
1.2 Applications

- LCD TV appliances
- High power inverter system
- LCDM appliances

1.3 Quick reference

- $BV \geq 40\text{ V}$
- $R_{DS(ON)} \leq 0.60\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- $P_{tot} \leq 300\text{ W}$
- $R_{DS(ON)} \leq 1.15\text{ m}\Omega @ V_{GS} = 6\text{ V}$
- $I_D \leq 400\text{ A}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)	 <p>Top View TOLL</p>	
2,3,4,5,6,7,8	Source(S)		
9	Drain(D)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _C = 25 °C	-	40	V
V _{GS}	Gate-Source Voltage	T _C = 25 °C	-	± 20	V
I _D ^{*,***}	Drain Current (DC)	T _C = 25 °C, V _{GS} = 10 V	-	400	A
		T _C = 100 °C, V _{GS} = 10 V	-	300	A
I _{DM} ^{*,**}	Drain Current (Pulsed)	T _C = 25 °C, V _{GS} = 10 V	-	1200	A
P _{tot}	Drain power dissipation	T _C = 25 °C	-	300	W
T _{stg}	Storage Temperature		- 55	175	°C
T _J	Junction Temperature		-	175	°C
I _S	Continuous-Source Current	T _C = 25 °C	-	400	A
E _{AS} [*]	Single Pulsed Avalanche Energy	V _{DD} = 40 V , L= 1.0 mH	-	1984	mJ
R _{θJA} [*]	Thermal Resistance- Junction to Ambient		-	40	°C/W
R _{θJC} [*]	Thermal Resistance- Junction to Case		-	0.5	

Notes :

- * Surface Mounted on 1 in² pad area, t ≤ 10 sec
- ** Pulse width ≤ 300 μs, duty cycle ≤ 2 %
- *** Limited by bonding wire

4. Marking Information

Product Name	Marking
UP006N04TH	

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UP006N04TH	TOLL-8L			2000	

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

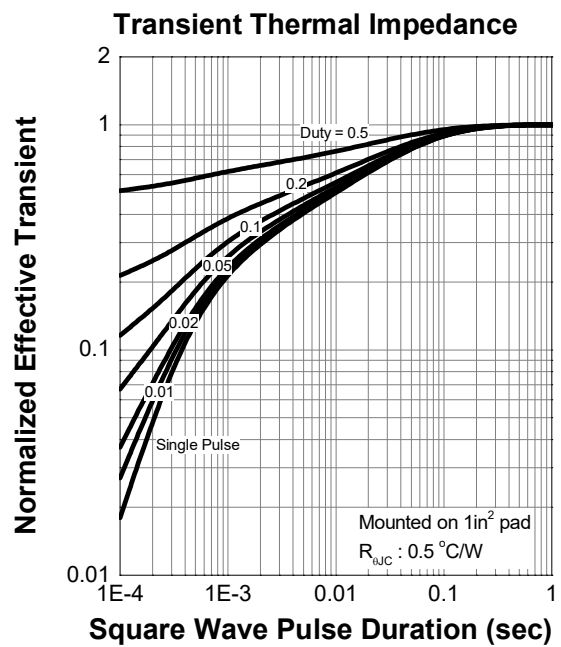
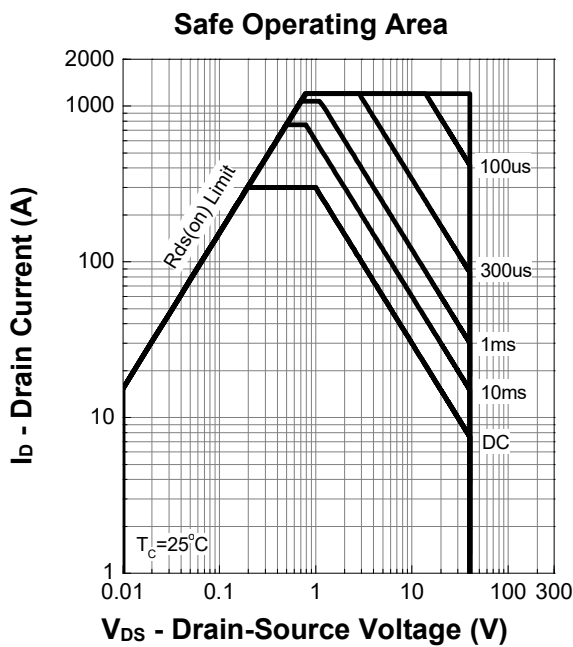
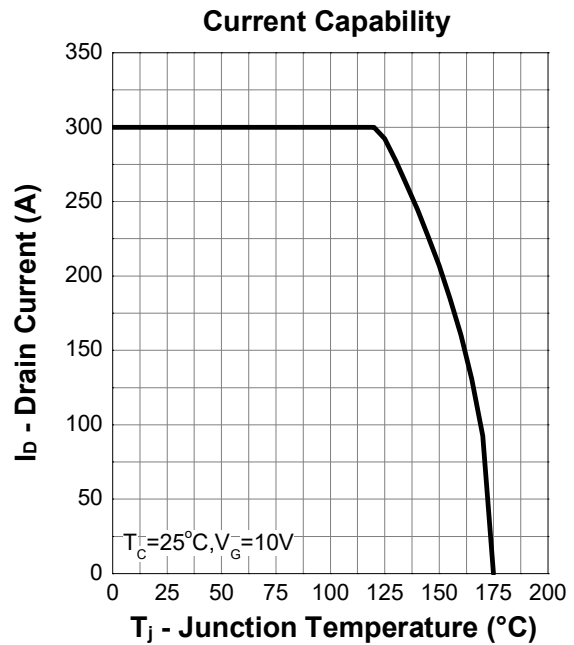
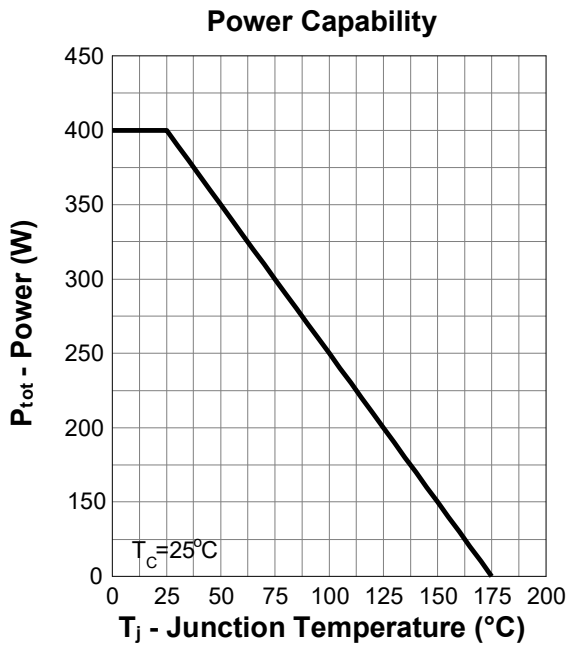
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	2	-	4	V
I_{DSS}	Drain Leakage Current	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA
$R_{DS(ON)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 80\text{ A}$	-	0.54	0.60	m Ω
		$V_{GS} = 6\text{ V}, I_{DS} = 40\text{ A}$	-	0.98	1.15	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 80\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_{DS} = 40\text{ A}, V_{GS} = 0\text{ V}$ $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	60	-	nS
Q_{rr}	Reverse Recovery Charge		-	61	-	nC
Dynamic Characteristics^b						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	8725	-	pF
C_{oss}	Output Capacitance		-	3774	-	
C_{rss}	Reverse Transfer Capacitance		-	116	-	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GEN} = 10\text{ V},$ $R_G = 3.9\ \Omega, R_L = 0.25\ \Omega,$ $I_{DS} = 80\text{ A}$	-	29	-	nS
t_r	Turn-on Rise Time		-	193	-	
$t_d(off)$	Turn-off Delay Time		-	91	-	
t_f	Turn-off Fall Time		-	144	-	
Gate Charge Characteristics^b						
Q_g	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 80\text{ A}$	-	145	-	nC
Q_{gs}	Gate-Source Charge		-	47	-	
Q_{gd}	Gate-Drain Charge		-	34	-	

Notes :

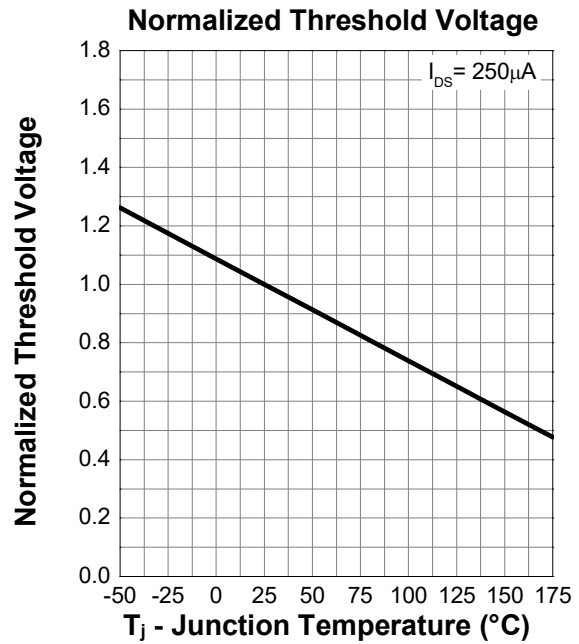
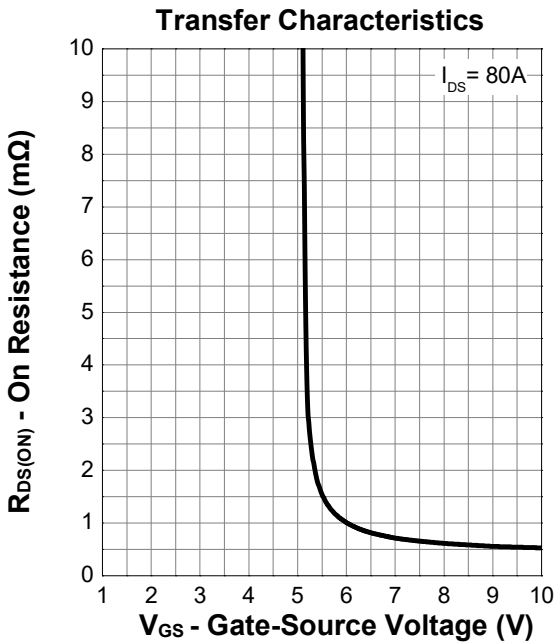
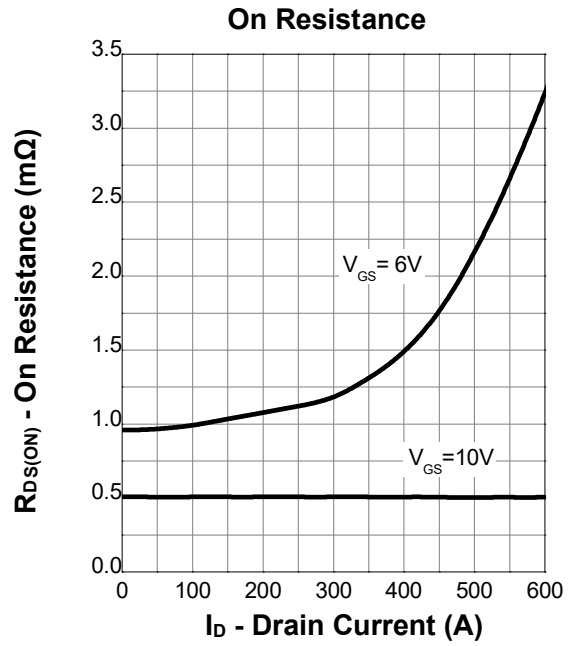
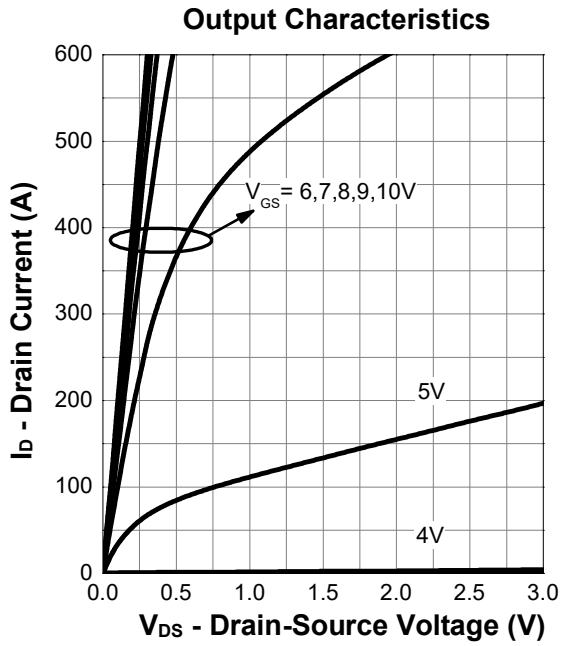
a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

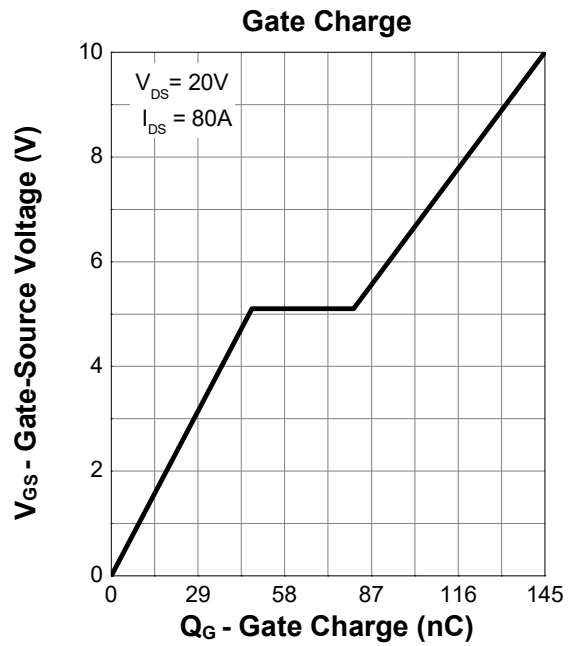
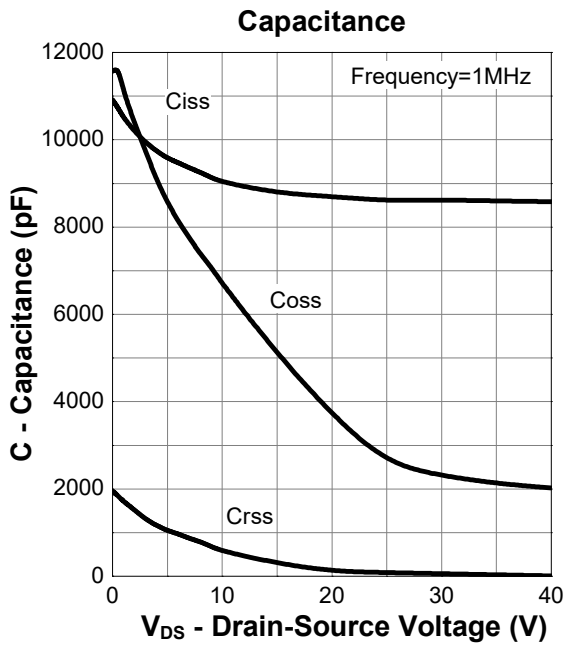
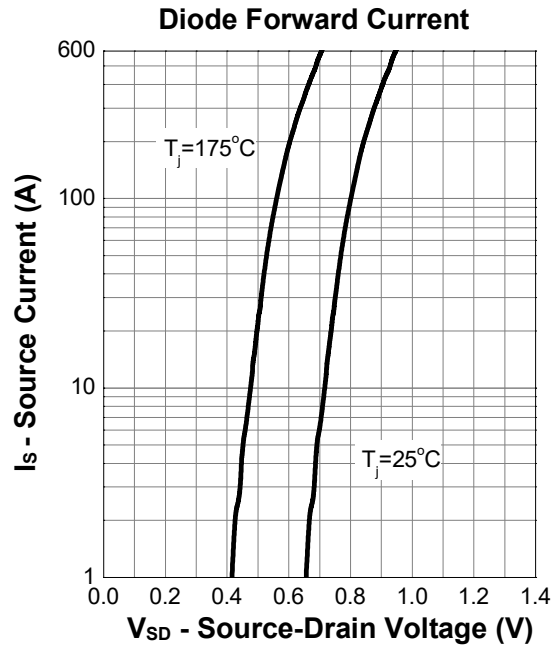
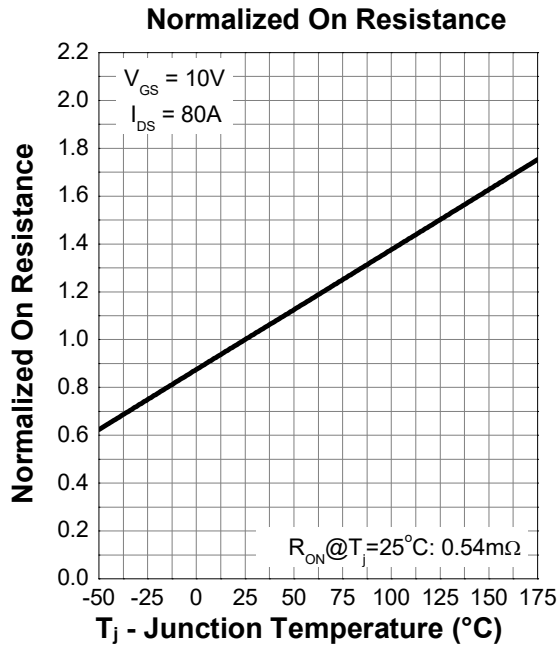
7. Typical Characteristics



7. Typical Characteristics (cont.)

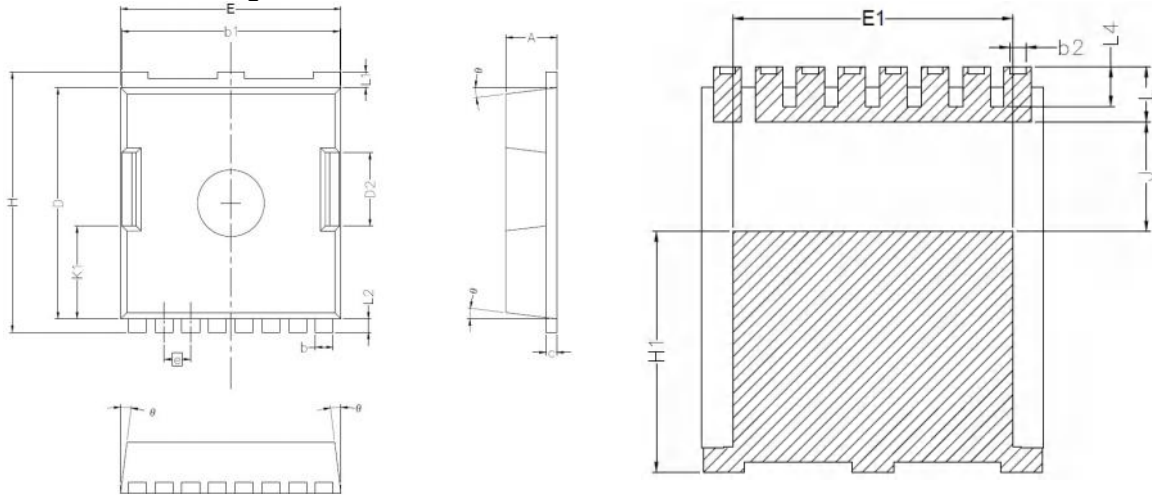


7. Typical Characteristics (cont.)



8. Package Dimensions

TOLL-8L Package



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°