N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Surface-mounted package
- ☑ MSL1
- ☑ Advanced trench cell design
- ☑ Tj Max 175℃

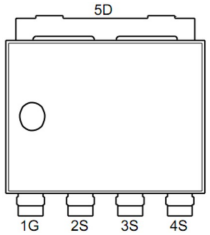
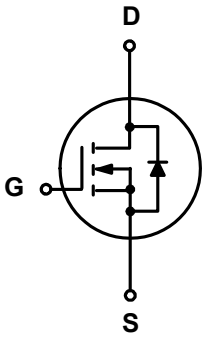
1.2 Applications

- ☑ Li-battey protection
- ☑ DC-DC
- ☑ High power inverter system

1.3 Quick reference

- ☑ BV ≧ 40 V
- ☑ P_{tot} ≦ 375 W
- ☑ I_D ≦ 715 A
- ☑ $R_{DS(ON)}$ ≦ 0.55 mΩ @ V_{GS} = 10 V
- ☑ $R_{DS(ON)}$ ≦ 1.50 mΩ @ V_{GS} = 6 V

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)		
2,3,4	Source(S)		
5	Drain(D)		

Top View

LFPAK88

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	-	40	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	±20	V
I_D*,***	Drain Current (Silicon limited)	T_C = 25 ℃, V_{GS} = 10 V		715	A
	Drain Current (DC)	T_C = 25 ℃, V_{GS} = 10 V	-	400	A
		T_C = 100 ℃, V_{GS} = 10 V	-	400	A
I_{DM}*,**	Drain Current (Silicon limited)	T_C = 25 ℃, V_{GS} = 10 V	-	2860	A
P_{tot}	Drain power dissipation	T_C = 25 ℃	-	375	W
T_{stg}	Storage Temperature		-55	175	℃
T_J	Junction Temperature		-	175	℃
I_S	Continuous-Source Current	T_C = 25 ℃	-	715	A
E_{AS}	Single Pulsed Avalanche Energy	V_{DD}=40V , L=1.0mH	-	3042	mJ
$R_{\theta JA}$**	Thermal Resistance- Junction to Ambient		-	43	℃/W
$R_{\theta JC}$	Thermal Resistance- Junction to Case		-	0.4	

Notes：

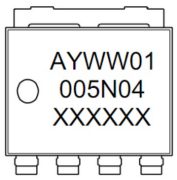
* Pulse width ≤ 300 μs, duty cycle ≤ 2 %

** Surface Mounted on 1 in^2 pad area, t ≤ 10 sec

*** Limited by bonding wire

**** Silicon limited

4. Marking Information

Product Name	Marking
UK005N04L8	

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
UK005N04L8	**LFPAK88**			**2000**	

6. Electrical Characteristics (T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	40	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = 0 V, I_{DS} = 250 μA	2	-	4	V
I_{DSS}	Drain Leakage Current	V_{DS} = 32 V, V_{GS} = 0 V	-	-	1	μA
I_{GSS}	Gate Leakage Current	V_{GS} = 0 V, V_{GS} = ± 20 V	-	-	±100	nA
$R_{DS(ON)}$[a]	On-State Resistance	V_{GS} = 10 V, I_{DS} = 50 A	-	0.5	0.55	mΩ
		V_{GS} = 6 V, I_{DS} = 30 A	-	1.3	1.50	
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = 50 A, V_{GS} = 0 V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_{DS} = 50 A, V_{GS} = 0 V dI_{SD}/dt = 100 A/μs	-	67	-	nS
Q_{rr}	Reverse Recovery Charge		-	77	-	nC
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 20 V Frequency = 1 MHz	-	10333	-	pF
C_{oss}	Output Capacitance		-	5136	-	
C_{rss}	Reverse Transfer Capacitance		-	195	-	
t_d(on)	Turn-on Delay Time	V_{DS} = 20 V, V_{GEN} = 10 V, R_G = 3.9 Ω, R_L = 0.4 Ω, I_{DS} = 50 A	-	30	-	nS
t_r	Turn-on Rise Time		-	45	-	
t_d(off)	Turn-off Delay Time		-	103	-	
t_f	Turn-off Fall Time		-	53	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 50 A	-	110	-	nC
Q_{gs}	Gate-Source Charge		-	35	-	
Q_{gd}	Gate-Drain Charge		-	12	-	

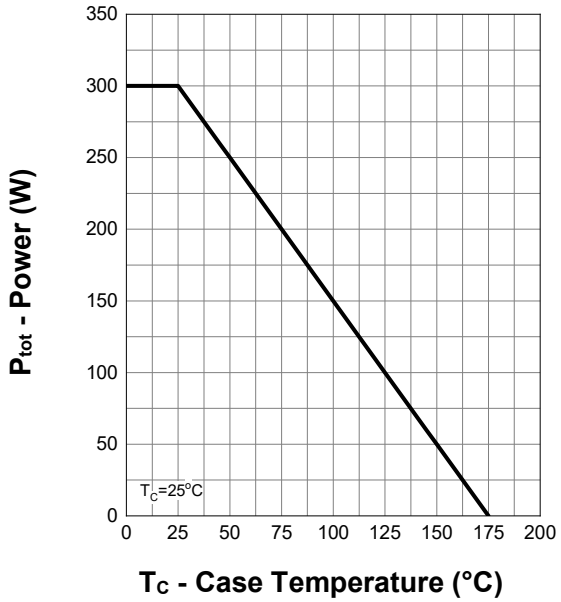
Notes：

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%

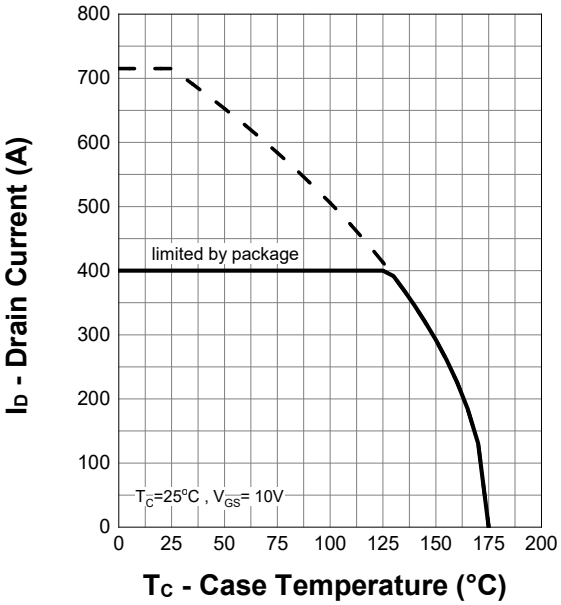
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

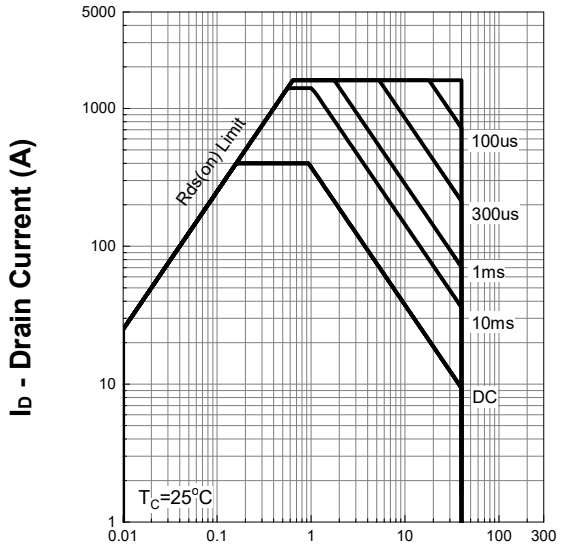
Power Capability



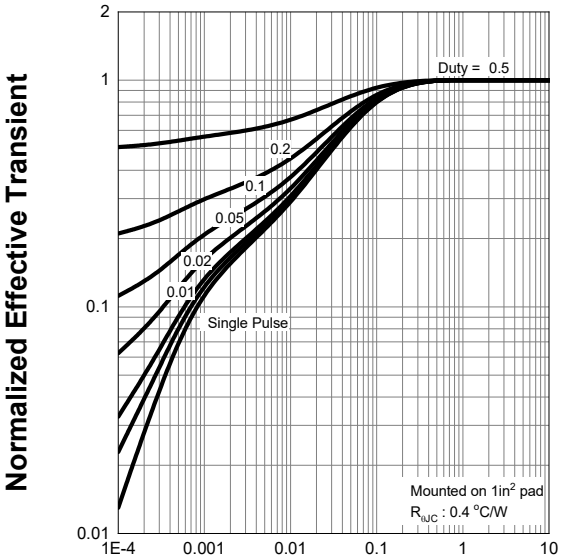
Current Capability



Safe Operating Area

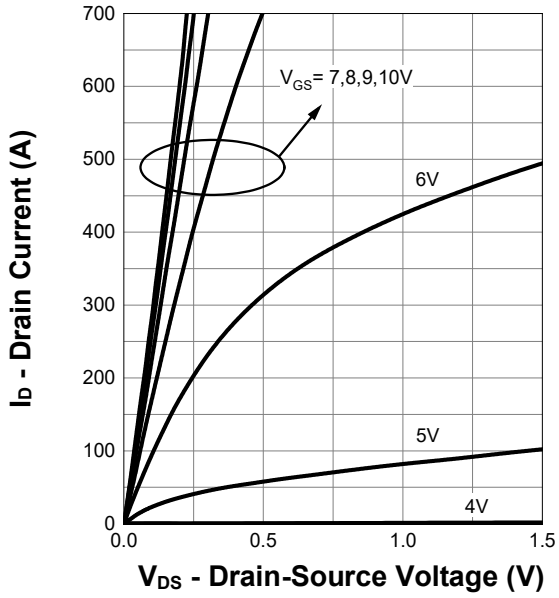


Transient Thermal Impedance

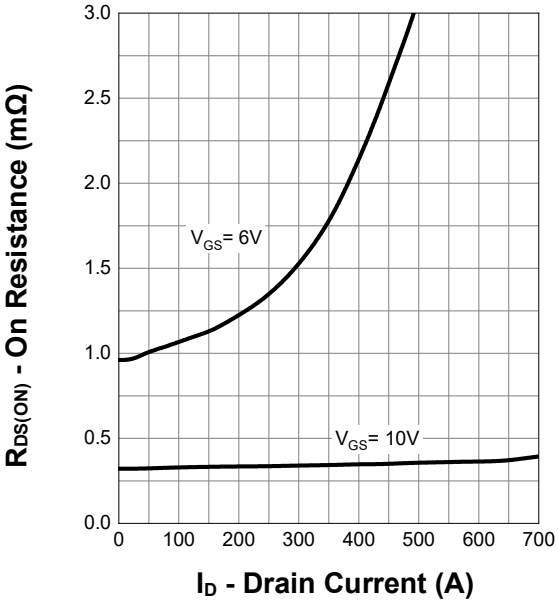


7. Typical Characteristics (cont.)

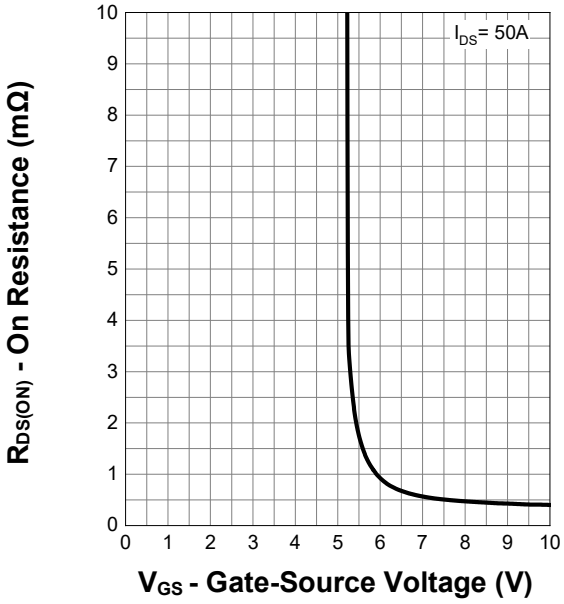
Output Characteristics



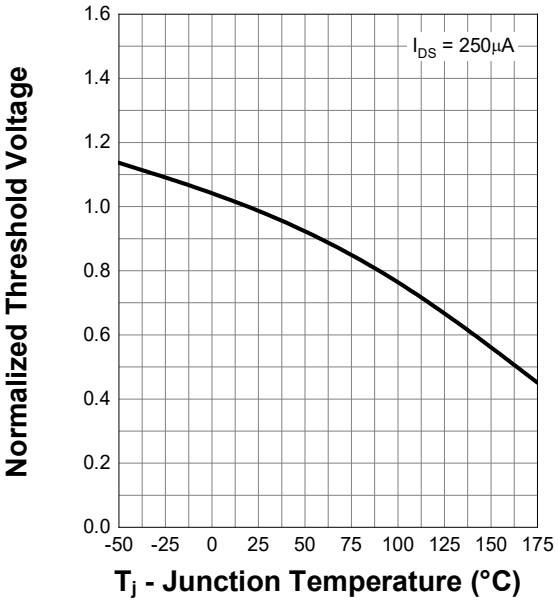
On Resistance



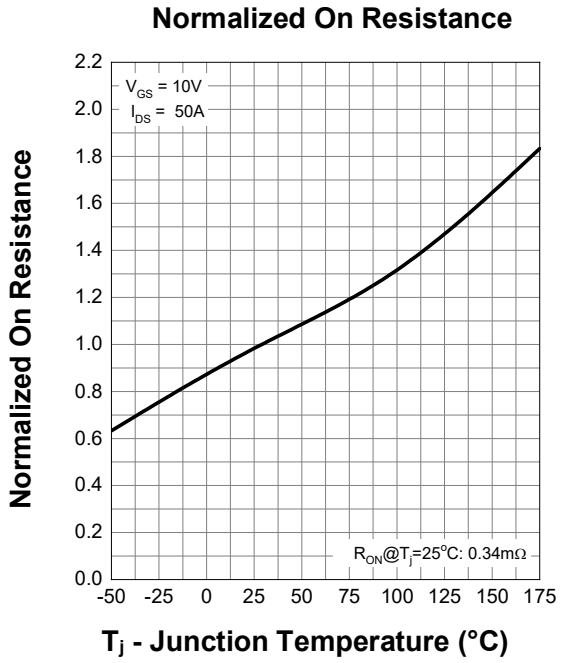
Transfer Characteristics

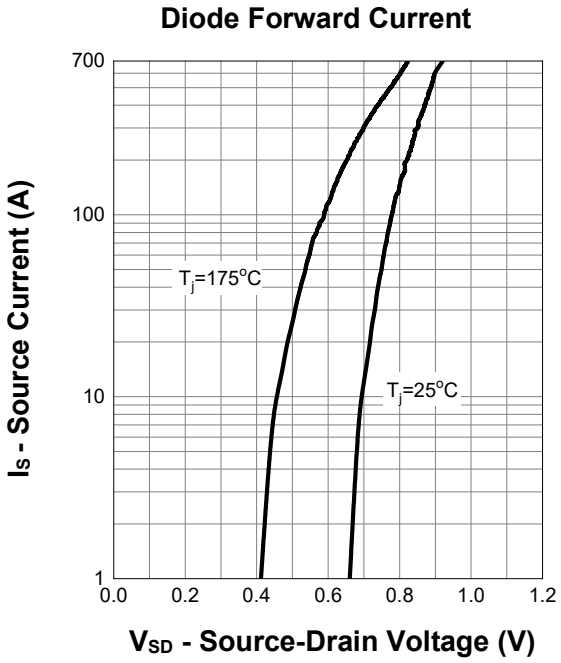


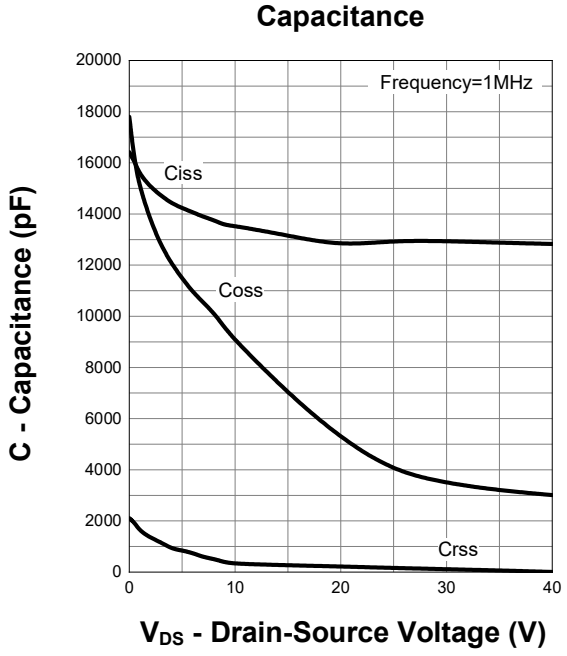
Normalized Threshold Voltage

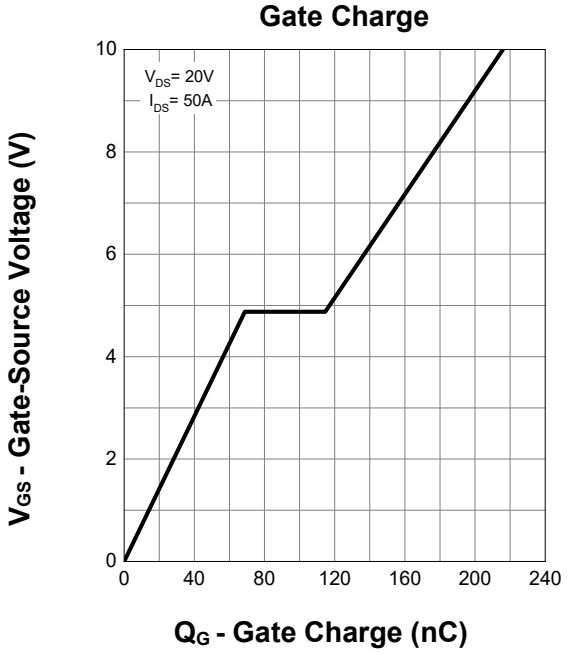


7. Typical Characteristics (cont.)









8. Package Dimensions

LFPAK88 Package